Electrical Transport Properties of N- and P- Doped InSe: Bulk Crystals versus Exfoliated Layers

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Abstract of Thesis

Electrical Transport Properties of N- and P- Doped InSe: Bulk Crystals versus Exfoliated Layers

Efficient doping of 2D materials, including carrier type, concentration, and mobility, is challenging but essential for enabling their future electronic and photonic applications. We are developing substitutional n- and p- doping of InSe semiconductor by introducing Sn and Zn, respectively, in the Bridgman bulk crystal growth.

Electrical transport properties of undoped vs. n- and p- doped InSe crystals are compared by conducting Hall measurements on bulk crystals and FET transport measurements on exfoliated thin layers. Undoped InSe is intrinsically n-type in both bulk and thin-film forms, with [n]~3.5E14 cm-3 and mu values of up to 1,400 cm2 V-1 s-1 for thick layers at 300K. Carrier concentration in Sn-doped thick layers increases approximately two-fold, while the corresponding mobility reduces ~2 times at 300 K. Zn-doped InSe shows p- behavior for bulk InSe with [p]~7.9E13 cm-3 and mu~43 cm2 V-1 s-1 at 300 K, which reverts to ambipolar/n-type behavior for thin layers in FET devices.

To get the most accurate field-effect mobility by InSe FET, we compare different methods of fabricated FET devices, introducing the PMMA coating layer and Electron Beam Lithography. By comparing different fabrication methods, we found that both the fabrication methods mentioned above help reduce the trapped charges of InSe channel and surface, also increase the stability and mobility value of FET.

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Chapter 1: Introduction

This chapter introduces the motivation of research on Indium Selenide, the current progress of device research on Indium Selenide, and research findings in this thesis.

1.1 Van-der-Waals Layered Materials

Since the first point-contact transistor be invented in 1947, silicon plays the most important role in the next 70 years. Until now, it still is the rudimentary element in the semiconductor industry. With the development of the semiconductor manufacturing process, the size of the transistor is getting smaller and smaller. So far, the process of the 7nm node has been commercialized. Moreover, the process of the Sub-5-nm node is already in development. Fig. 1.1 shows the roadmap of the scaling down of transistors, which presents the stacked devices and 3D devices will be the future devices. On the other side, with the scaling of size, the performance of silicon transistors is getting close to its physical limits [1][74]. In order to solve the predictable bottlenecks in the semiconductor field, finding another substitutable semiconductor material with better performance has become an urgent challenge.

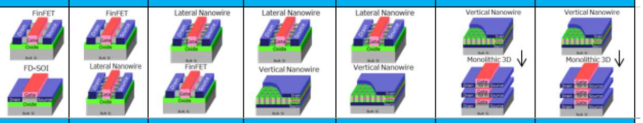
YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14T2	P32M14T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5-f1.0	i1.0-f0.7
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA 3DVLSI	VGAA, LGAA 3DVLSI
Logic device mainstream device	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
DEVICE STRUCTURES							
							
LOGIC TECHNOLOGY ANCHORS							
Patterning technology inflection for Mx interconnect	193i, EUV	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV+(DSA)	193i, High-NA EUV+(DSA)	193i, High-NA EUV+(DSA)
Channel material technology inflection	Si	SiGe25%	SiGe50%	Ge, IIIV (TFET?), 2D Mat	Ge, IIIV (TFET?), 2D Mat	Ge, IIIV (TFET?), 2D Mat	Ge, IIIV (TFET?), 2D Mat
Process technogy inflection	Conformal deposition	Conformal Doping, Contact	Channel, RMG	Stacked-device Non-Cu Mx	Stacked-device Non-Cu Mx	Steep-SS, 3D	Steep-SS, 3D
Stacking generation inflection	2D	2D	3D-stacking: W2W D2W	3D-device: P-over-N Hetero	3D-device: Mem-on-Logic Hetero	3D-device: Mem-on-Logic Hetero	3D-device: Logic-on-Logic Hetero

Fig. 1.1. Device Roadmap Enabling More Moore Scaling from IRDS 2017 [56]

The Van-der-Waals layered materials provide a promising direction for the future electronics field. The most appealing property of layered materials is that it exhibits excellent functional electronic characteristics when the thickness of the material under a few layers. Graphene, the best-known Van-der-Waals layered materials, was first discovered since 2004. [57] Until now, graphene sill is the most popular research topic in the field condensed matter physics [10], biomedical devices [11], semiconductor devices [2][75][76][77], and other many nanomaterials-related research fields. Graphene is a single sp2-bonded carbon atoms layer. Moreover, the lattice of graphene is a honeycomb shape [12]. After first single-layer graphene by exfoliated by Ander Geim, many promising devices based on graphene have been achieved, including flexible transparent electrodes [13]; RF circuits [14]; electrochemical electrodes [15][16]; tunable plasmonic devices [17]; heterostructure in electronic devices [18][78][79].

After the discovery of single-layer graphene exhibiting extremely high electron mobility of 200,000 cm2/V·s [2], researchers surprisingly found the family of Van-der-Waal layered materials providing a promising direction for scaling down the size of the future transistor, because of the inherent advantage of atomic thickness in the vertical size of 2D materials devices. Considering the absence of a bandgap in graphene [58], the transition metal dichalcogenides family is a good candidate for building FET devices. Typical TMD materials present the form of MX2, where M represents a transition metal, such as Mo, W, Nb, and X, represents the elements from chalcogens, includes S, Se, Te. MoS2, a typical TMD Van-der-Waal layered material, has been proven to be a promising semiconductor material in recent years [59][80]. Fig. 1.2 shows the crystal structure of MoS2. It could be used to build large-scale digital circuits above a flexible and transparent

substrate, and also could be used as sensing materials and building digital signal processing circuits for biosensors [19][20][21]. The group of TMD layered materials provides diverse electronic and optical properties [3][4][5]. The monolayer of MoTe2 exhibits the property of phase transition from the 2H phase to 1T′ phase under electrostatic doping [22]. The monolayer of NbSe2 presents the property of superconductivity [23]. Benefiting from the discovery of these special physical properties, TMD layered materials opens up the possibility for engineers to develop more creative electronics devices. After a lot of experimental proofs and processing technology research, TMD layered materials can gradually provide a good technical reserve for future electronic devices and optoelectronic devices.

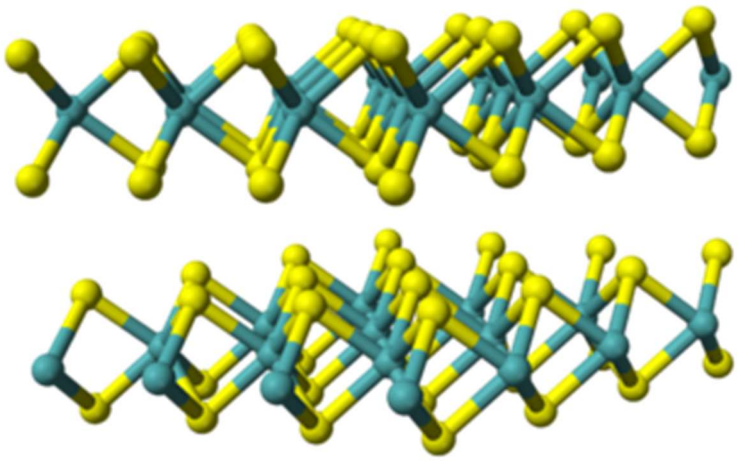


Fig. 1.2. Crystal Structure of Molybdenum Disulfide

In addition to TMD layered materials, there are other types of Van-der-Waal layered materials, including III-VI Van-der-Waals layered materials, such as GaSe, InSe, In2Se3, and III-V Van-der-Waals layered materials, such as hBN. III-VI semiconductor materials have been used as photoelectric and photovoltaic materials since the 1980s because of the

direct bandgap [24]. Recently, the paper reported by Ander Geim renews the attention to III-VI Van-der-Waals layered materials, the single layer of Indium Selenide, as a semiconductor material with a 1.28eV bandgap at monolayer, exhibiting electron mobility of more than 1000 cm2/V·s at room temperature [8].

hBN, the typical III-V layered material is a good insulator layer for devices of Van-der-Wall layered materials because of a large bandgap (5.9eV) [25]. Fig. 1.3 shows the crystal structure of a typical III-V insulator, hBN. The planar hexagonal lattice structure of hBN, which is similar to graphene, makes it sufficiently stable and inert. And, hBN has an atomic-level smooth surface and zero dangling bonds or surface charge traps because of zero out-of-plane atoms [7].

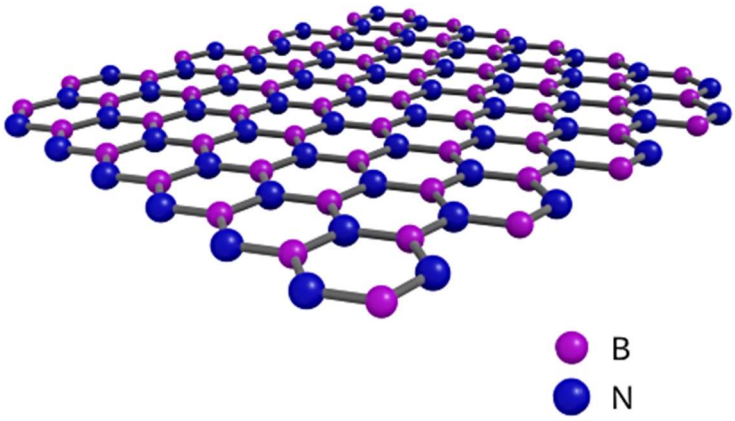


Fig. 1.3. Crystal Structure of hexagonal Boron Nitride

1.2 InSe Crystal Structure

As shown in figure 1.4, each layer of InSe is stacked by four monoatomic layers in the sequence of Se-In-In-Se [60]. And In each monoatomic layer, atoms are arranged in the same plane as the shape of hexagon. In a single layer of InSe, all atoms are connected

by covalent bonds. And the bonding between adjacent layers is Van-der-Waals force [26][27].

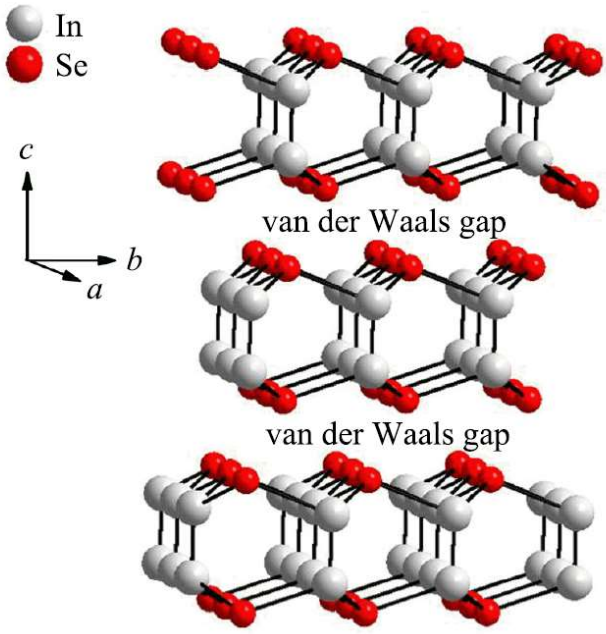


Fig. 1.4. Crystal Structure of InSe staked by three layers

Wieting and Schluter firstly reported there are three different polytypes of InSe crystal structure, including β, ϒ, ε polytypes, as shown in Fig. 1.5 [28][31]. All polytypes have similar hexagonal plane when projected to the 2D plane. The difference of three polytypes comes from stacking sequences and lateral placement of adjacent layers [28][29]. In three polytypes, the β and Ɛ polytypes have the same lattice parameters (a = 4.05 Å and c = 16.93 Å) and belong to the hexagonal system with eight atoms extended over two layers in each unit cell [61]. The ϒ polytype InSe has a Rhombohedral unit cell structure, with a lattice parameter (a = 4.002 Å and c = 24.961 Å), which contains three layers InSe [30].

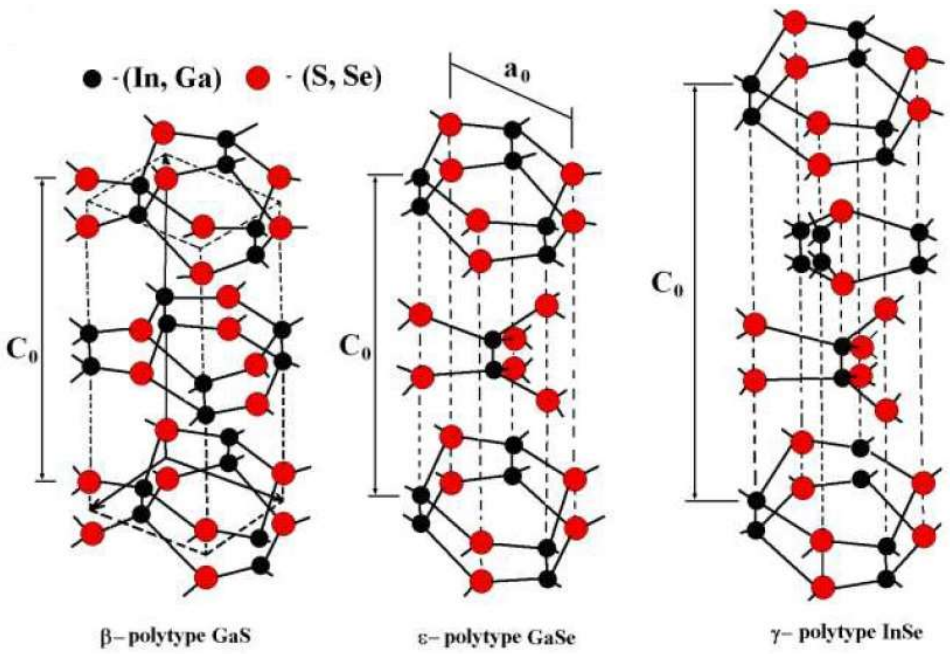


Fig. 1.5. crystalline structure and layer stacking for various crystal polytypes of group [62]

For identification of crystal structure of ϒ-polytype InSe and β and Ɛ polytypes, Mudd et al. concluded the experiment demonstration by matching Raman Spectra data with reference[30]; Kovalyuk et al. analyzed the data of ϒ-polytype InSe X-ray diffraction and matching the Raman Spectra data with reference [32]; Kuroda et al. firstly analyzed Raman Spectra data to prove the ϒ-polytype InSe [33].

Besides the analysis of the XRD spectrum and Raman Spectrum, Transmission electron microscopy (TEM) provides visualized and intuitive analysis to identify ϒ-polytype InSe with β, ε polytype InSe. One reason is the lattice parameters β, ε polytype is different from the lattice parameter of ϒ-polytype. For distinguishing other two types polytype InSe, β, ε, Chen et al. reported the spatial frequency of β, ε polytype InSe for the first reflections is 0.294 Å-1, which is fitted to the 100 diffraction spot of β, ε polytypes

InSe. In the ϒ-polytype, the first observable reflection should be (100), corresponding to the spatial frequency of 0.5 Å-1. However, discrimination of β polytype and ε polytype is severe by TEM because of the same lattice parameters. According to group theory, the β and ε polytypes are invoked by the various groups, a non-symmorphic D_{6h}^{4} group for β polytype and a symmorphic D_{3h}^{1} group for ε polytype. Thus, the Raman spectrum can discriminate the β and ε polytype by checking a mode around 200 cm-1 which is present in the ε polytype but absent in the β polytype [34][35].

1.3 InSe Physical Properties

1.3.1 Electronic Properties

In three polytypes, the β and ϒ polytypes have a direct band gap with closely values [26],1.28eV [61] and 1.29eV [63], respectively, and the ε polytype InSe has an indirect band gap of 1.4eV [26]. Due to the quantum confinement effect, the ϒ polytype shows the interesting point that the bandgap is exhibiting the direct-indirect transition when thickness decreasing from bulk to a few-layer and monolayer [64]. According to DFT calculation, the bandgap values for 1L, 3L, 5L and bulk are 2.84eV, 1.98eV, 1.84eV and 1.29eV, as shown at Fig. 1.6 [52].

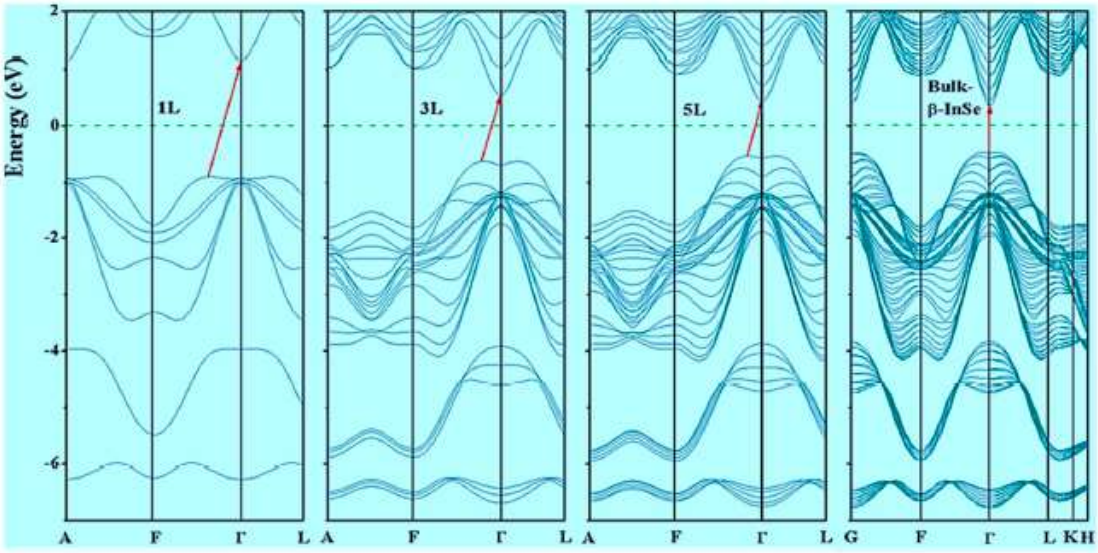


Fig. 1.6. Electronic band structures of β-InSe, 1L, 3L, 5L and bulk crystal. [52]

In Fig. 1.6, the minimum point of conduction band (CBM) appears at the Γ point, and the maximum of the first valence band (VBM) appears at a point along the Γ-F direction. The two peaks (the so-called sombrero-shape dispersion) at edge of valence band enhaves the probability of electron transfer between the valence band and conduction band in monolayer and few-layer. Moreover, there exist more than one valence band maxima and conduction band minima in almost the same momentum vector, thus electronic allowed transition can take place in these extrema via optical absorption. On the other hand, the band dispersions observed in monolayer, few-layer and bulk are similar and attributed to uniform crystallinity but the dispersions intensity are quite not the same and this link to thickness dependency [52]. In summary, the bandgap dependence on layer thickness offers tunability of the bandgap as well as the corresponding associated electronic properties.

1.3.2 Optical Properties

To further understand the direct-indirect property of InSe, the photoluminescence (PL) spectrum has been investigated by researchers. Fig. 1.7 indicates the PL spectrum for InSe

crystals using laser excitation at photon energies of 2.3, 2.7, and 3.8 eV [8]. In this figure, the PL spectrum of 2-8 layers InSe shows two peaks, A peak at a lower energy and B peak at higher energy. And monolayer InSe only shows the peak at high energy. And the blueshift of A peak at lower energy was found with decreasing of layer numbers.

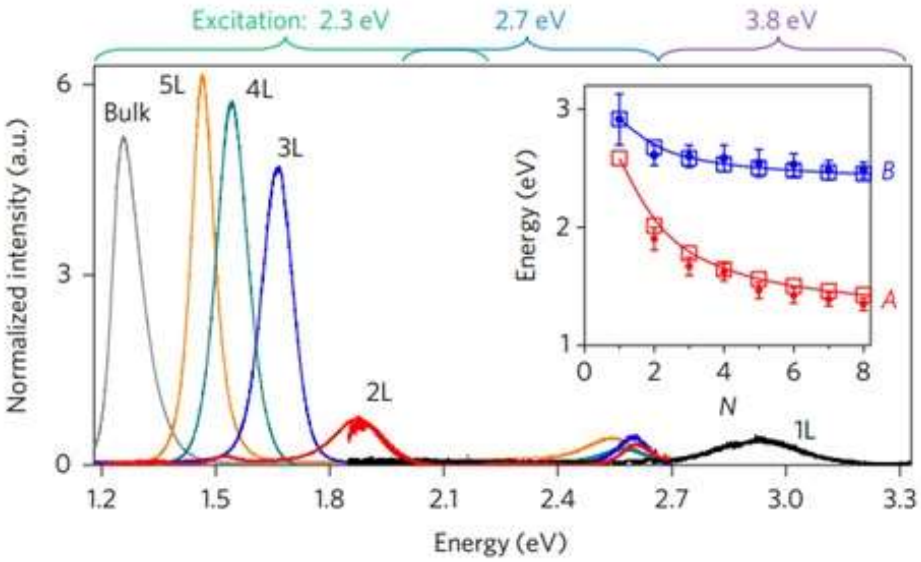


Fig. 1.7 Photoluminescence of InSe measured at room temperature for bulk InSe and thin layer InSe [8].

Combining with the DFT calculation, the observed decrease in the PL energies with increasing N can be explained as follows. The electronic bands of 1 layer InSe split into N subbands in the N-layer crystal, and this reduces the energy difference between the conduction and valence states in the vicinity of the Γ point at which the bandgap is smallest [66]. The leads to a decrease in the principal bandgap that give rise to the A peak. A smaller reduction occurs for the B peak that involves deeper, less-affected valence bands [8].

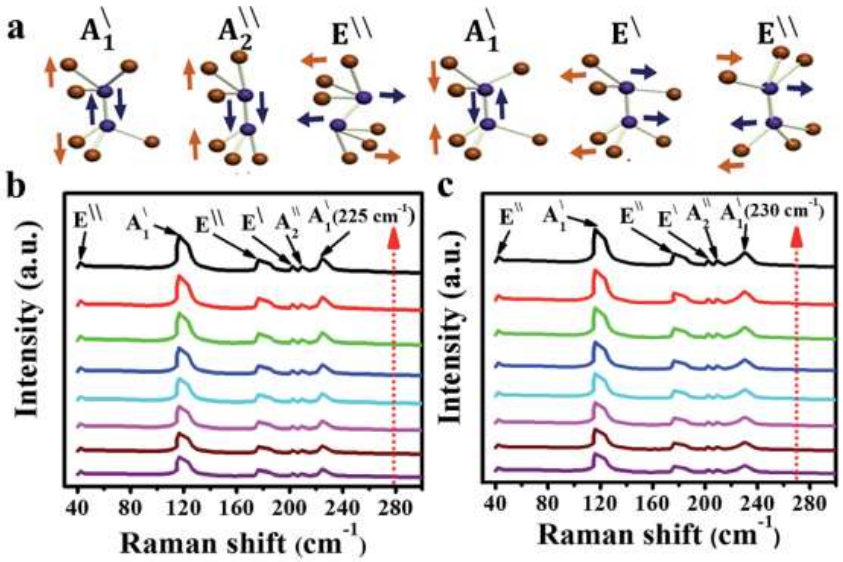


Fig. 1.8 a). Schemes of the six Raman modes of InSe. b). Raman spectra of thickness dependency. c). Raman spectra of annealed flakes as a function of thickness dependency. [53]

Carlone C. et al shows the layered InSe belongs to a D_{6h}^{4} symmetry and has six Raman modes [35]. The six modes are shown in Fig. 1.8a. In Fig. 1.8b, the six modes are classified as E'' at 41 cm-1, A'1 at 117 cm-1, E'' at 176 cm-1, E' at 202 cm-1, A''2 at 209 cm-1 and A'1 at 41 cm-1, the thickness from bottom to top in both b and c are 6, 9, 11, 13, 15, 18, 21 and 24 nm [53].

1.4 The Carrier Mobility Measurement of InSe

1.4.1. The Hall Mobility of Indium Selenide

Due to the great potentials for electronic and optoelectronic applications, the mobility of InSe have been intensively studies in the past years. In the bulk form, the hall mobility of InSe could be near 1,000 cm2/(V·s) at room temperature and higher than 10,000 cm2/(V·s) at 60 K [68], making it a promising semiconductor material to build high

performance transistor. Segura A. et al reported the temperature and magnetic field dependence of electron Hall mobility and magnetoresistance coefficient in n-type InSe (GaS doped and Sn-doped) [67]. In the thin film form, more recently, Bandurin et al reported a electron gas in few-layer InSe encapsulated in hexagonal boron nitride under an inert atmosphere, where carrier mobility exceed 103 cm2/(V·s) at room temperature and 104 cm2/(V·s) at liquid-helium temperatures, respectively [8].

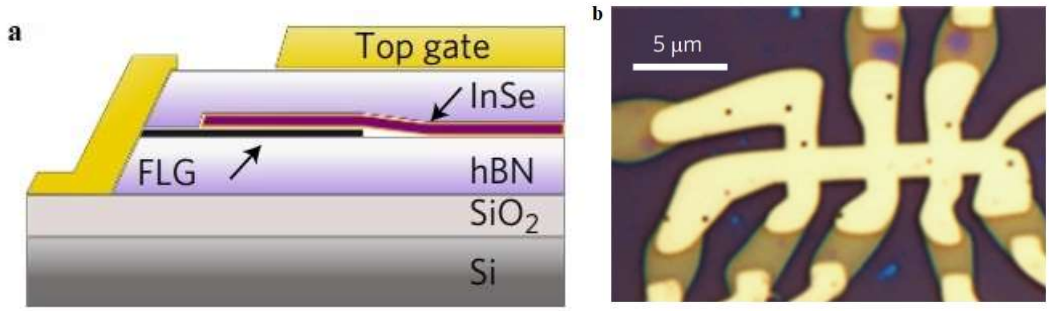


Fig. 1.9 a). Cross-sectional schematic of device of few-layer InSe encapsulated in hexagonal boron nitride. b). Optical image of a device, The central bright area is the top gate that covers the encapsulated InSe. Peripheral Au contacts lead to hBN-encapsulated few-layer graphene that is not covered by the top gate; the few-layer graphene region is dark yellow [8].

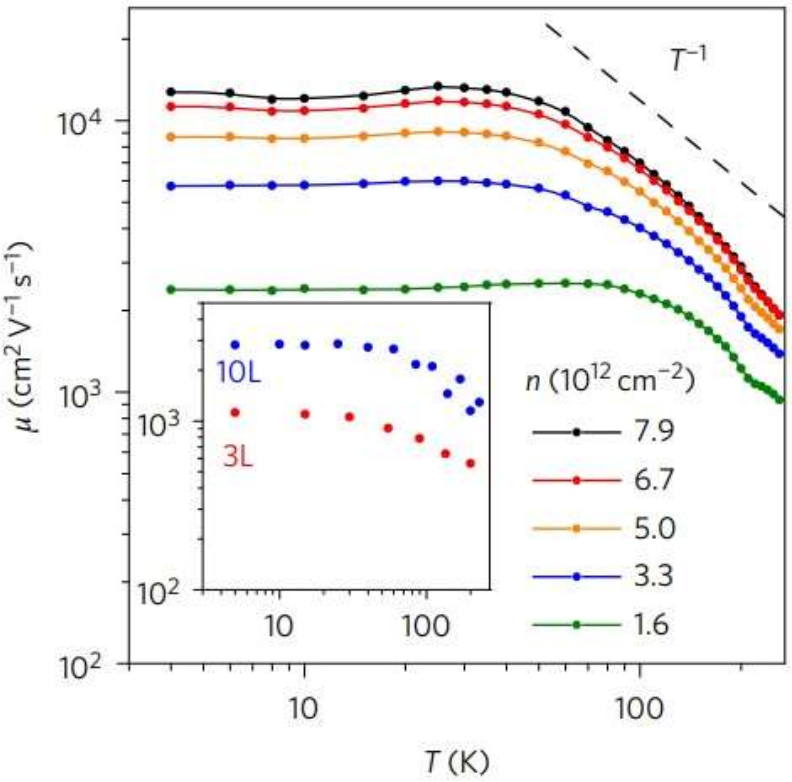


Fig. 1.10 Temperature dependence of the Hall mobility μ for the 6-layers device. The dashed black line shows the dependence expected for acoustic phonons. Inset: μ(T) for 3-layers and 10-layers at high doping (8.3 and 7.7 × 10^{12} cm^{-2}, respectively) [8].

As shown at figure 1.9, the mechanically exfoliated InSe flake was transferred onto a hBN flake prepared on a SiO2 wafer. Followed that, Few-layer graphene was positioned on top of the hBN serve as electrical contacts to the InSe flakes. All of the structure was then covered with a second hBN crystal to completely isolate InSe from the environment. Whole devices were etched through the top hBN, InSe and Few-layer graphene to define Hall bars. Finally, Au/Cr contacts to graphene were deposited. The top hBN flake served as the dielectric layer for the top gate whereas the SiO2/Si wafer acted as the bottom dielectric/gate electrode [8].

As shown in figure 1.10, the mobility shows the dependency as a function of

temperature. The different color lines represent the different electron density n in InSe flakes doped by the top and bottom gate voltages. Below 50K, μ is almost independent of T by electron disorder (Anderson localization). For the T > 100K, the mobility μ decrease as the slope of T-1 attributed to acoustic phono scattering. At room temperature, μ drops to 103 cm2/(V·s), which is higher than the highest mobility reported for 2D dischalcogenides and comparable to that of black phosphorus [8].

1.4.2. Field-effect Mobility based InSe FET Devices

Some recent works also explored the field effect mobility of few-layer InSe by fabricating InSe FET devices [36][40][41][42][69]. And they improved the field effect mobility of few-layer InSe by using the Al2O3 as dielectric layers [42], modifying the interface between InSe flakes and dielectric materials [41] and screening the charge doping from air by PMMA coating [40]. The PMMA coated devices shows ultrahigh field effect mobility of InSe around 1,000 cm2/(V·s) which is approaching the Hall mobility value in the bulk form [40][69].

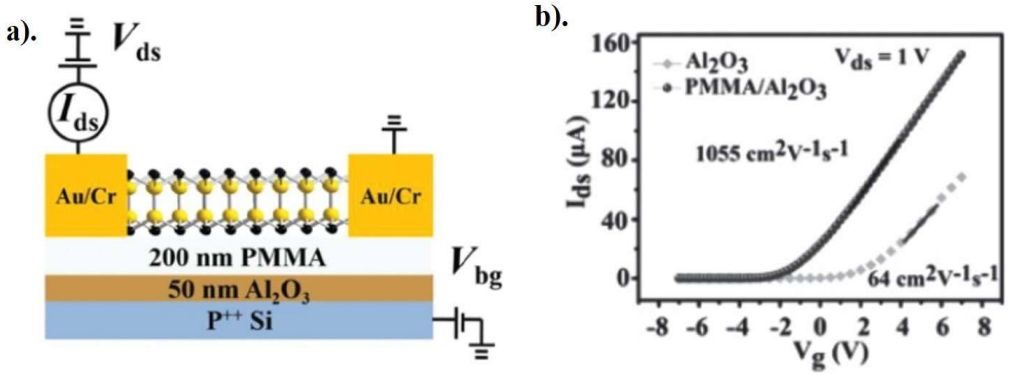


Fig 1.11 a). Schematic structure of back-gate multilayer InSe FET, PMMA/Al_2O_3 as the dielectric layer. Au/Cr electrodes (40/20 nm). b). Transfer curve of back-gate multilayer InSe FET, the dielectr layer is Al_2O_3 and PMMA/Al_2O_3, respectively [69].

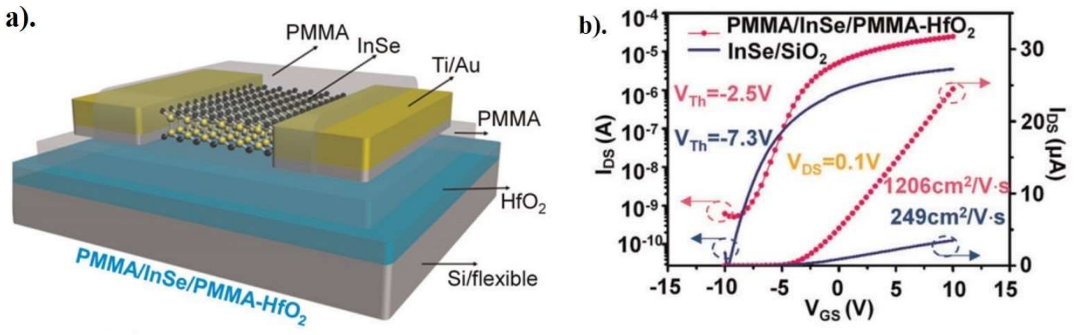


Fig. 1.12 a). Schematic diagram of back-gate multilayer InSe FET, PMMA/HfO_2 as the dielectric layer and Coated by PMMA layer. b). Transfer curve of PMMA/InSe/PMMA-HfO_2 and InSe/SiO_2 FET [36].

As shown in figure 1.11 and figure 1.12, to investigate the field effect mobility and transistor behavior of multilayer InSe, the back-gate devices were fabricated on the dielectric layer of PMMA/Al2O3 or PMMA/HfO2. These structures improve the field effect mobility in multilayer InSe FET devices to 1000 cm2/(V·s). PMMA coating layer plays a key role of suppressing the interfacial coulomb impurities at interface of oxidized dielectric substrate [69].

1.5 Outline of My Thesis

This main goal of this thesis is to investigate the electrical transport property of InSe by measuring both the hall mobility and field-effect mobility at bulk form and thin-film form, respectively. Especially, we investigated the performance change of Field-effect Transistor (FET) dependent on the flake thickness, dielectric layer thickness and interfacial charge doping.

Firstly, we grew undoped InSe, Sn-doped InSe, and Zn-doped InSe single crystals by Bridgman method. We characterized the grown material X-ray powder diffraction

(XRD), Transmission Electron Microscopy (TEM), photoluminescence (PL) spectroscopy, and Raman spectroscopy. Then, we used the Hall Effect Measurement System to investigate the Hall effect mobility of InSe in bulk sample at room temperature. Moreover, we fabricated the multilayer InSe FET devices by mechanically exfoliating. we analyzed the FET behavior of multilayer InSe and studied the performance change affected by layer thickness, dielectric layer thickness and interfacial charge doping.

The thesis is organized as follows:

In chapter 2, we will illustrate the Bridgman growth method and the detailed process of the growth of InSe, also including the growth process of Sn-doped InSe and Zn-doped InSe. Next, we utilize the XRD spectra, PL spectra and Raman spectra to analysis and the crystal structure parameters, energy band diagram and verifying the polytype of our sample. Further, the TEM images presents the legible picture of crystal structure and the distribution of atoms. Finally, we will mechanically exfoliate InSe flakes in different thickness and measure the thickness by Atomic Force Microscope. We will compare optical images of flakes with the AFM image and understand the color dependency of flakes thickness. AFM characterization is a preparation of fabricating FET devices, which would help us choose flakes with right thickness.

In chapter 3, we will measure the mobility of InSe bulk crystal by Hall Effect Measurement, as called Hall effect mobility. We prepare three samples of different doped InSe, including undoped InSe, Sn-doped InSe and Zn-doped InSe, respectively. The thickness of them are between 200-500 μm regarded as bulk form, comparing with the thickness of multilayer InSe film. We calculate the carrier density, conductivity and Hall mobility by measuring the Hall voltage. By comparing the results of different doped InSe,

we analysis the effect of dopants on the electron transportation of InSe. Last but not least, we conduct the Hall Effect Measurement at low temperature by using Physical Property Measurement System (PPMS) to investigate the temperature dependency of electron transportation of InSe. The phonon scattering mechanism of InSe will be explored.

In chapter 4, we mainly acquire the Field Effect mobility of multilayer InSe by measuring the InSe FET. We also get the on/off ratio, threshold voltage and on-status current level by analyzing the Output Curves and Transfer Curves. Back-gate multilayer InSe FET is fabricated and analyzed at NIST CNST and GWNIC. For improving on-status current and reducing the contact resistance, we try both methods of Photolithography and Electron Beam Lithography (EBL). For reducing the hysteresis loop, we try 285nm, 90nm and 50nm SiO2/Si substrates. For suppressing the surface charge doping, we coat the PMMA layer as the protection layer. Final, we discuss the thickness dependency of FET behavior.

In chapter 5, a summary and conclusions are presented. Future work to further optimize the performance of multilayer InSe FET, including improving the value of on-status current, the on/off ratio.

Chapter 2: Crystal Growth and Materials Properties

2.1 Single Crystal Growth

In our experiments, InSe single crystals are grown by the vertical Bridgman-Stockbarger method. This method includes melting of polycrystalline material sealed in an evacuated quartz ampoule followed by a translation of the ampoule along the temperature gradient in the furnace as illustrated in Fig. 2.1. Solidification of the melt begins at the tapered end of the ampoule when it cools down below the melting point (Tm). A very slow translation speed of the ampoule (typically >1 mm/h) provides quasi-equilibrium crystallization of the melt resulting in a single-crystalline ingot of the material.

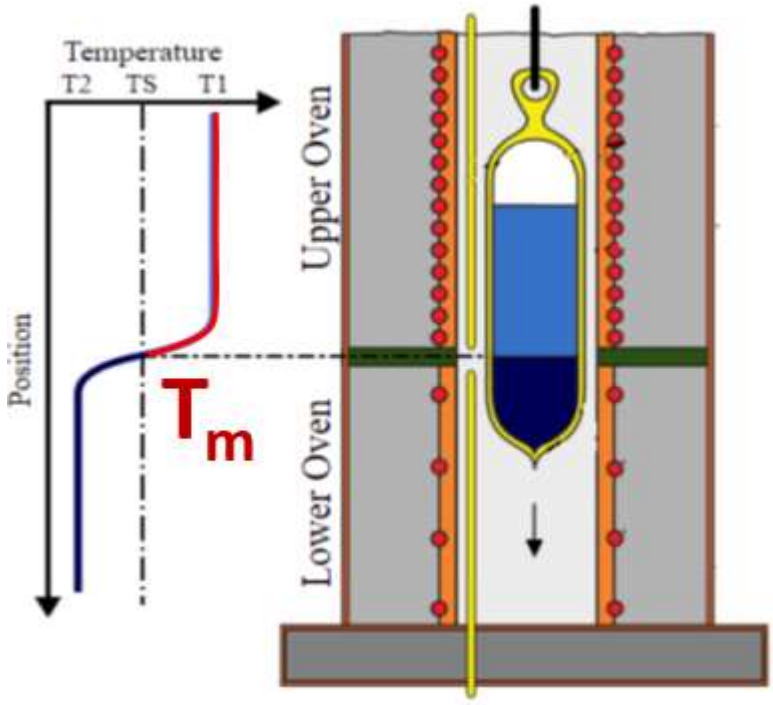


Fig. 2.1 Schematic diagram of Bridgman-Stockbarger growth

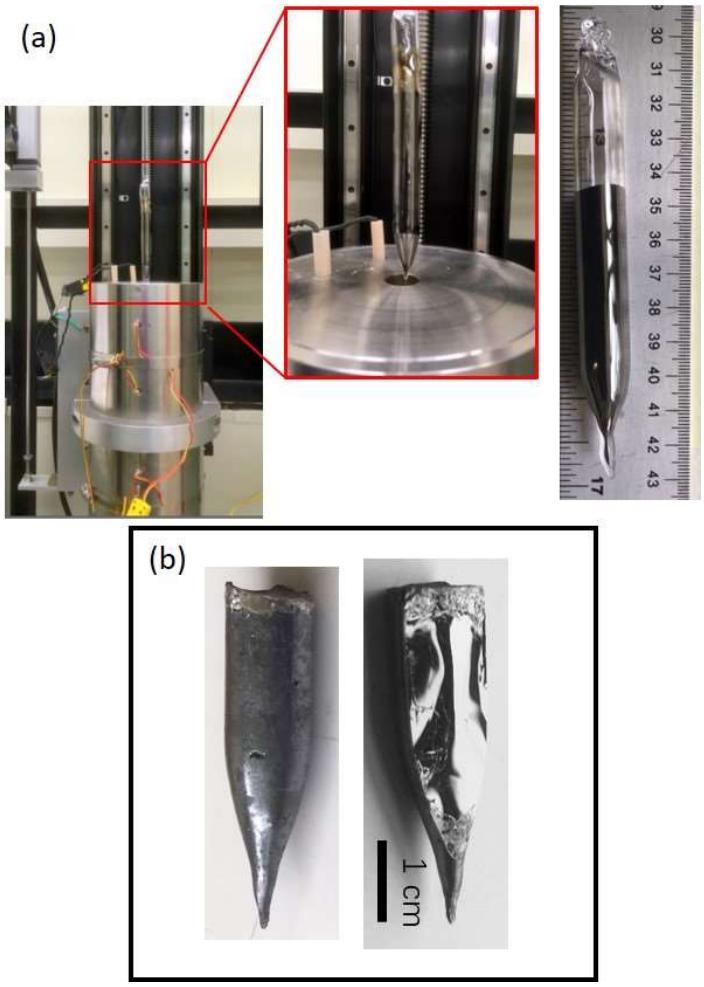


Fig. 2.2 (a) Bridgman growth setup at NIST, including a graphitized ampoule with polycrystalline InSe charge used to obtain a single-crystalline InSe ingot shown in (b). Panel (b) also shows the InSe ingot after cleavage parallel to the c-plane.

Here, we present the detailed growth process of InSe single crystal. Firstly, polycrystalline InSe charge was synthesized by reacting In (99.99%) and Se (99.99%) mixed in proportion In : Se = 52% : 48% in a graphitized quartz ampoule at 720 °C for 8 h. A non-stoichiometric starting mixture was adopted based on literature that reported that using an In-rich charge results in an increased yield of the InSe phase due to avoiding the peritectic decomposition of InSe during cooling of the melt. The obtained poly-InSe was

milled and loaded in another ampoule that was graphitized by acetone pyrolysis (Fig. 2.2 (a)). The ampoule was sealed under vacuum and placed in a vertical furnace. Before the growth, the InSe charge was kept at 720 °C for 3 h to homogenize the melt. Then, the molten charge was moved through a thermal gradient at a rate of 0.5 mm/h.

As shown in Fig. 2.2(b), a 3.5 cm long, 1 cm in diameter InSe ingot was obtained. XRD measurements confirmed that the ingot is mostly pure InSe with only top ~3 mm being close to In2Se3. XRD and high-resolution TEM studies revealed that InSe produced in our experiment crystallized as the ε polytype (space group symmetry D_{3h}^{1}) that is characterized by a hexagonal lattice consisting of eight atoms in the unit cell, and their extension over two layers.

Nominally undoped InSe always exhibits n-type conductivity. In order to further increase electron concentration, we grew Sn-doped InSe. Sn dopant in the form of elemental Sn (1.3 at. %) was added during synthesis of poly-InSe. Similarly, p-type InSe was obtained by Zn-doping using ZnSe powder. For the p-InSe samples studied in this work, Zn concentration in the melt was 0.3 at. %.

2.2 X-ray Diffraction and TEM analysis of crystal structure

For the powder XRD study, InSe single crystal was finely ground using an agate mortar. The XRD patterns were collected on Norelco Philips Diffractometer in the Bragg-Brentano geometry using the Cu K-α radiation. Lattice parameters were refined using the MDI-JADE 6.5 software package (Materials Data Inc., Livermore, CA 2015). XRD scan in Fig. 2.3 shows that InSe crystallizes in hexagonal ε-structure, space group P-6m2 (187), with the lattice parameters a= 4.008(3) and c=16.651(2) Å.

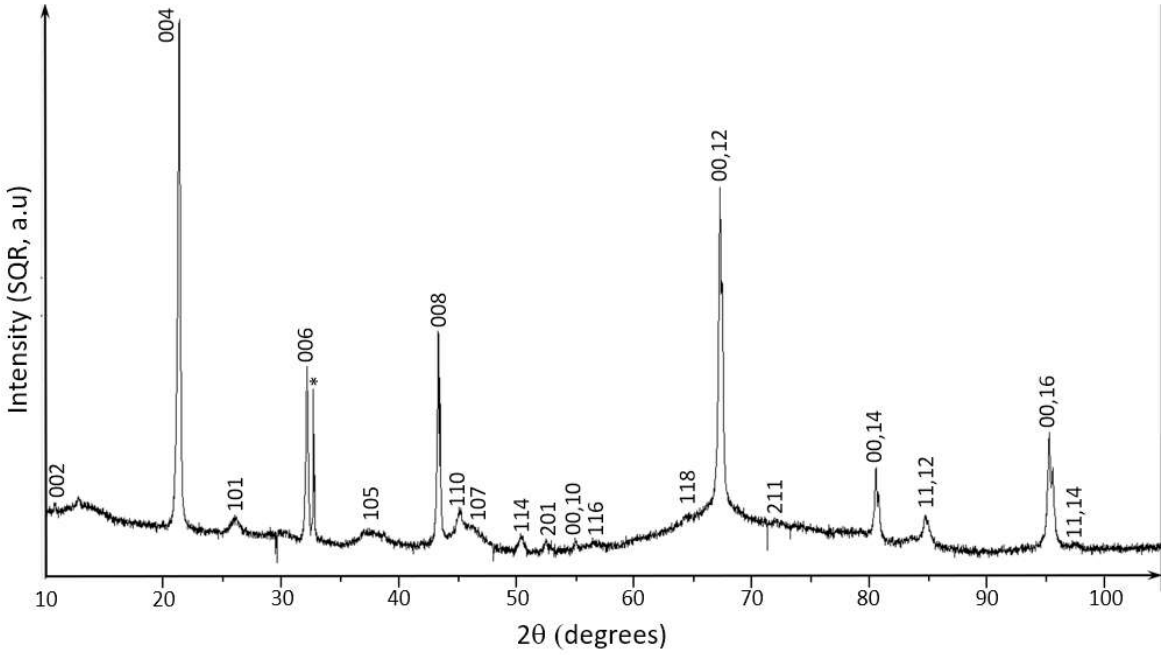


Fig. 2.3 Powder XRD pattern of ε-InSe crystal with assigned hkl values

The crystal structure of ε-InSe was further verified by performing transmission electron microscopy measurements. An Aberration-Corrected High Angle Annular Dark Field Scanning Transmission Electron Microscopy (Cs-corrected HAADF-STEM) FEI Titan 80-300 TEM/STEM operating at 300kV was employed for the characterization of single-crystalline InSe flakes. The flakes were crushed in ethanol and a drop of solution was deposited onto a TEM grid. Fig 2 shows STEM image of few-layer thick InSe flakes in (0001) orientation with the atomic model for the ε-InSe crystal structure in the inset.

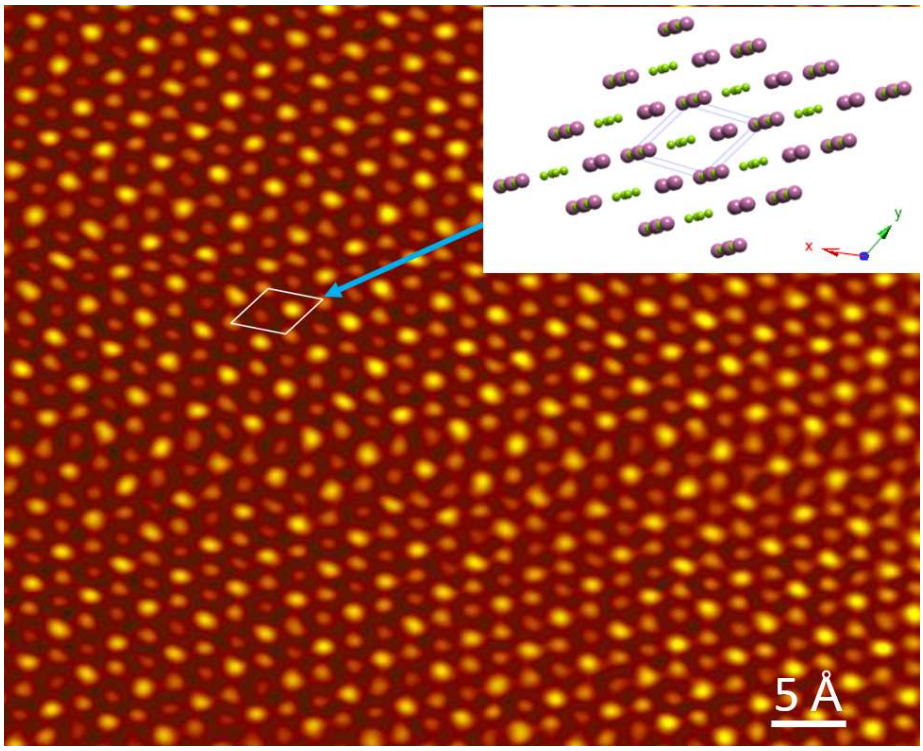


Fig. 2.4 HAADF-STEM image of (0001)-oriented ε-InSe layers with the corresponding atomic model in the inset, where In and Se atoms are dark-red and green spheres, respectively (courtesy of Dr. Huairuo Zhang, NIST)

2.3 Raman and Photoluminescent properties

For van der Waals layered materials, Raman spectroscopy is a very important characterization technique to identify the vibration modes and crystal structure. In InSe, the inter-valence-band transition E' (from px,py-like orbitals to the conduction band) has an energy of about 2.40 eV[72] therefore using a 514.5 nm (2. 41 eV) laser allows to detect more vibrational lines due to the quasi-resonant excitation. In each unit cell of Ɛ-InSe, there are two layers of Se-In-In-Se atomic unit, 8 atoms in each unit; as a result, it has 24 vibration modes. Because of the D3h symmetry, Ɛ-InSe has four A2' modes, four A1'

modes, eight E' modes and eight E'' modes. Figure 2.5 shows the vibrational modes that were identified in the literature.[26]

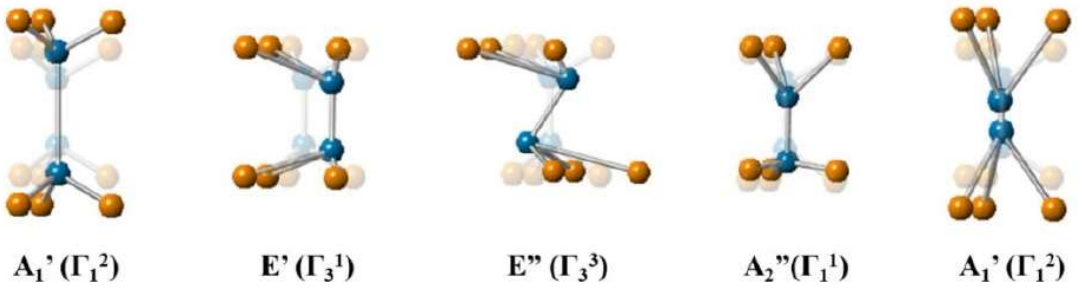


Fig. 2.5 The active Raman modes in InSe crystal.[26]

In our experiments, Raman spectra of exfoliated InSe flakes were recorded at room temperature using a resonant (514.5 nm) and non-resonant (633 nm) excitations, as shown in Figure 2.6 and Figure 2.7, respectively. In the resonant Raman spectrum, we observed fours peaks at the 114.6 cm-1, 176.9 cm-1, 198.0 cm-1, 226.7 cm-1, which correspond to A1', E'(LO)+E'', A''(LO), and A1' modes, respectively. These four peaks are the most typical peaks for the Ɛ-InSe polytype observed in the literature[26,73]. The non-resonant Raman spectrum obtained from the 633 nm laser only shows 114.9 cm-1, 176.9 cm-1, 226.7 cm-1 peaks, which corresponds to A1', E'(LO)+E'', and A1' modes.

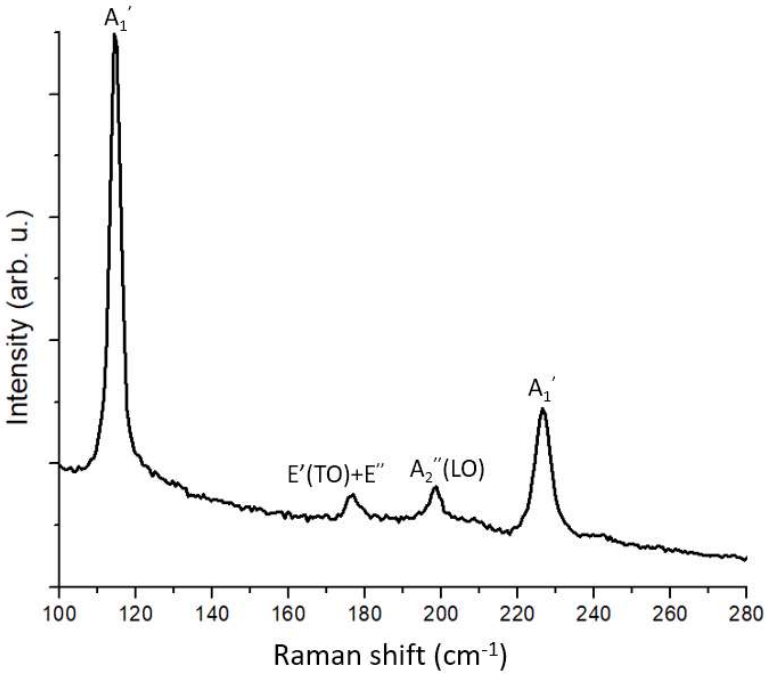


Fig. 2.6 Resonant Raman spectra of InSe exfoliated layers with the 515 nm laser excitation (Courtesy of Dr. Amber McCreary, NIST)

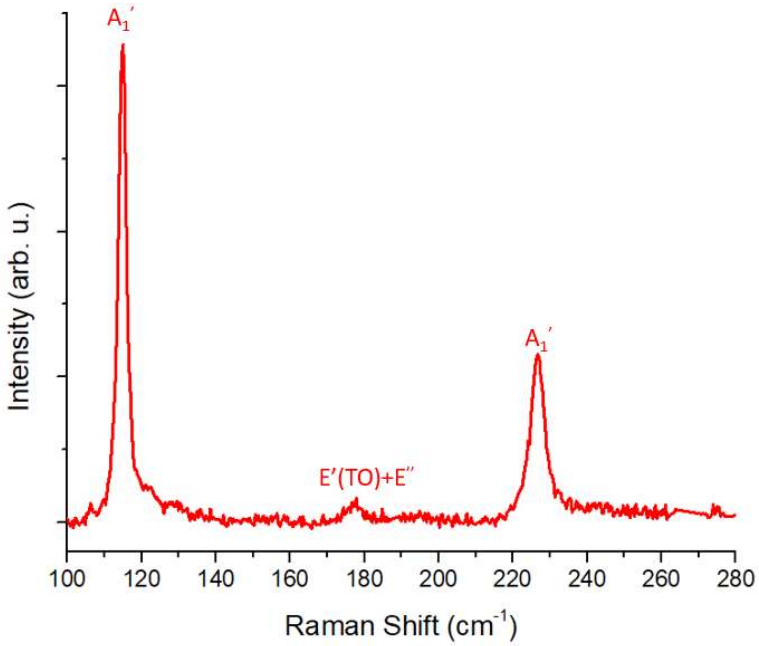


Figure 2.7 Non-resonant Raman spectra of InSe exfoliated layers with the 633 nm laser excitation. Note the absence of the A2’’(LO) mode at 198 cm-1 (Courtesy of Dr. Amber McCreary, NIST)

Thus, Raman spectroscopy confirmed that the synthesized material is indium monoselenide.

Chapter 3: Transport Properties of Bulk Crystal

Hall effect measurement is a typical method to characterize the transport and conductivity properties of materials. The two most essential parameters, mobility and carrier density, of semiconductor materials can be extracted by hall effect measurement. On the other side, at low temperatures, the acoustic phonon scattering will be suppressed. By observing the dependency of mobility and temperature, the transport property of InSe will be accurately investigated.

3.1 Hall Effect Mobility

In semiconductor materials, when a magnetic field is applied, the carriers (including electrons and holes) will experience a force, Lorentz force. Without the Lorentz force, the transport of carriers is controlled by the electrical field. And, the direction of carrier movement is along to the direction of applied electrical field. When a magnetic field is applied in a direction perpendicular to the direction of carrier movement, the direction of carrier motion will be deflected because of the simultaneous action of the electric field force and the Lorentz force, perpendicular to the electric field force. The total force is F, equal to q (E + v × B). q is the elementary charge, E is the electric field, v is the carrier velocity, and B is the magnetic field.

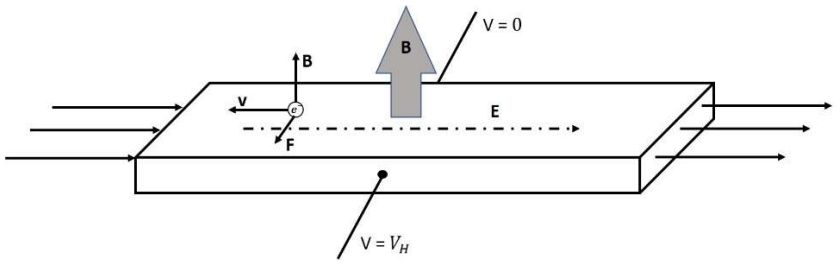


Fig. 3.1. the Hall bar shape of n-type semiconductor

For Fig. 3.1, in the n-type materials hall bar sample, as the majority carrier, electron subject to the Lorentz force and arrive at/in the front side of the sample, forming a negative surface on the front side of the sample. The charge accumulation will cause the potential difference in the direction of the unapplied voltage. This potential difference is the Hall voltage VH, and VH = IB/qns, where I is current, B is the magnitude of the magnetic field, d is the sample thickness, and q is the elementary charge. ns is the sheet carrier density, and ns = nd, n is the bulk carrier density. Thus,

$$n_s = \frac{IB}{q|V_H|}$$

The sheet density could be determined by measuring the Hall voltage VH, and the known values of B, I, and q. Because the majority of carriers in n-type and p-type semiconductors are electrons and holes, respectively, the hall voltage is negative for n-type and positive for p-type.

Moreover, to determine the hall mobility, the sheet resistance needs to know. Van der Pauw resistivity measurement can be used to accurately extract the resistance of Hall bar samples. The format formula is,

$$\mu = \frac{|V_H|}{R_s IB} = \frac{1}{qn_s R_S}$$

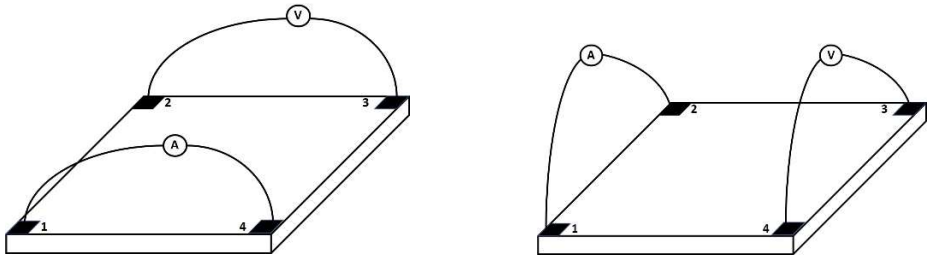


Fig. 3.2. The schematic of Hall Effect Measurement

In Van der Pauw's measurement, the two characteristics of resistance are extracted by the four-terminal sample. As shown in Fig. 3.2, two resistances, Ra = V14/I23, Rb = V34/I12 are related to extract the sheet resistance Rs by the Van der Pauw measurement. The equation

$$\exp(-\frac{\pi R_a}{R_s}) + \exp(-\frac{\pi R_b}{R_s}) = 1$$

For more accurately measuring the resistance and Hall voltage, there are some strategies. About the measurement of resistance, and combined with the Fig. 3.2,

$$R_{21,34} = V_{34}/I_{21},\ R_{12,43} = V_{43}/I_{12},$$
$$R_{32,41} = V_{41}/I_{32},\ R_{23,41} = V_{14}/I_{23},$$
$$R_{43,12} = V_{12}/I_{43},\ R_{34,21} = V_{21}/I_{34},$$
$$R_{14.23} = V_{23}/I_{14},\ R_{41,32} = V_{32}/I_{41},$$

In this table, although the right part of measurements is just a repetition of the left part after reversed voltage, it will allow the check of ohmic contact quality and sample uniformity. There are two criteria to judge the reliability of the data.

$$R_{21,34} = R_{12,43}$$
$$R_{32,41} = R_{23,14}$$
$$R_{21,34} = R_{34,21}$$
$$R_{21,34} = R_{41,32}$$

$$R_{21,34} + R_{12,43} = R_{32,41} + R_{23,14}$$
$$R_{21,34} + R_{34,21} = R_{21,34} + R_{41,32}$$

After verifying the reliability of data, the resistivity calculation formula,

$$R_a = \frac{R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21}}{4},$$

$$R_b = \frac{R_{32,41} + R_{23,14} + R_{43,12} + R_{34,21}}{4},$$

The sheet resistance Rs can be concluded by Van der Pauw equation, by using the above formula.

The measurements procedure includes,

First, apply a positive magnetic field

Apply a positive magnetic field B, apply a constant current from terminal 1 to 3, measure V42, Apply a constant current from terminal 3 to 1, measure V24. In same way, measure the V13, and V31.

Second, apply a negative magnetic field

In the same way as above, measure the V13, V31, V24, V42 again.

3.2 Room Temperature Mobility

To measure the Hall mobility of InSe bulk crystal, Hall-bar structure similar to Fig. 3.2 is fabricated. The sample is clave from a grown-InSe single crystal. And four terminals were welded by Indium metal. Fig. 3.3 shows the two samples of Sn-doped InSe and Zn-doped InSe.

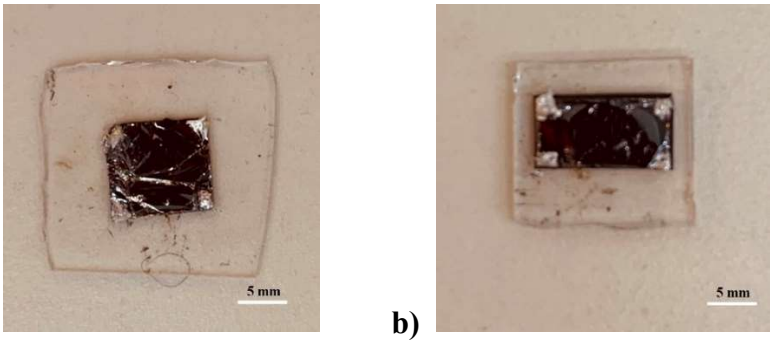


Fig. 3.3 a) Sn-doped Hall sample. b). Zn-doped Hall sample

The measurement system is HMS-5500 Hall effect measurement systems. As shown in the below picture, the four gold probes are connected to the four terminals of the hall sample.

a).

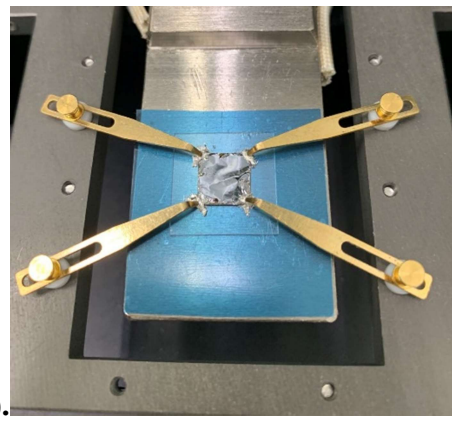
b). 

Fig. 3.4 a) Ecopia Hall Effect Measurement System. b). undoped-InSe hold on measurement system HMS-5500

To investigate the situation of ohmic contact quality and sample uniformity of fabricated samples, we conduct the resistance measurement. Sweeping the current from -70μA to 70μA, -100μA to 100μA, -2μA to 2μA for undoped InSe, Sn-doped InSe and Zn-doped InSe, respectively, the V-I graph shows at Fig. 3.5 (a, (b, (c. The variation of the sweeping range is dependent on the value of materials resistance. To fully observe the

ohmic contact quality, we need to the sweeping current range as much as possible within the limit of voltage from system setting, because too small sweeping current range will mislead the fact of Schottky contact. Under the investigation, the contact quality of Sn-doped and Zn-doped samples show good contact quality because of the similar value of Rab, Rbc, Rcd, Rad. There is a variation for the undoped InSe sample, which is considered as the nonuniform of material because the contact quality looks good and shows the behavior of Ohmic contact.

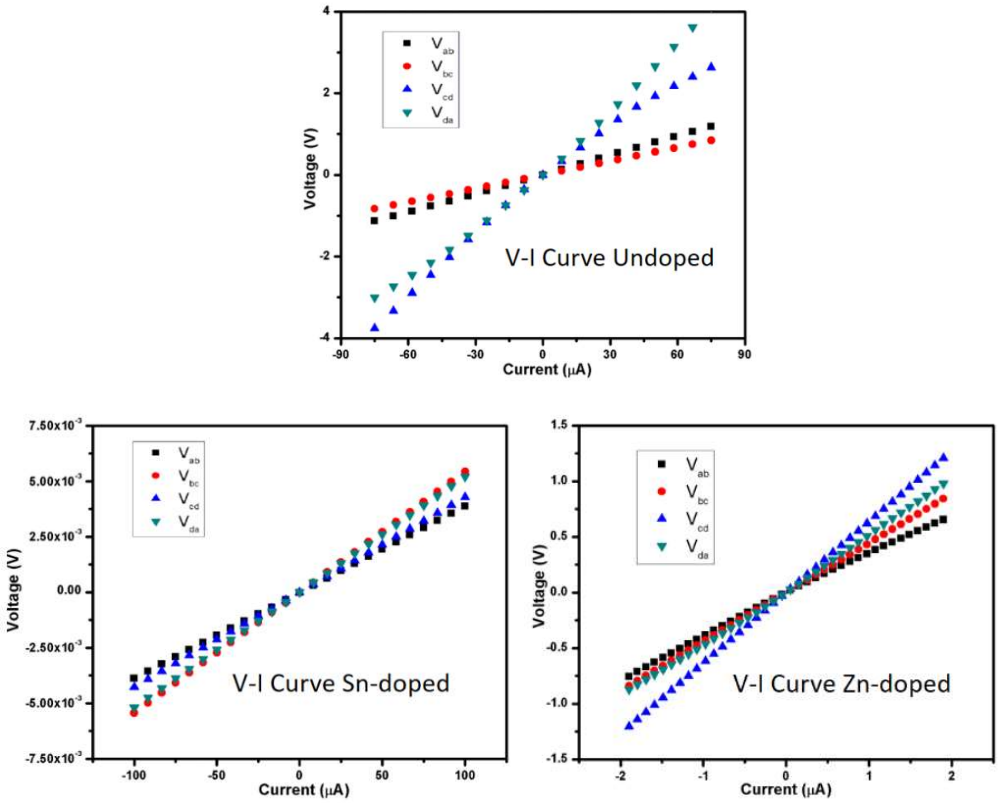


Fig. 3.5. The V-I curve of undoped InSe, Sn-doped, Zn-doped for measuring the contact quality.

After verifying the contact quality, we measure the carrier density and mobility of samples. This is the summary table of the tested sample. The negative value of bulk concentrations of undoped and Sn-doped InSe represents the carrier type of them is the

electron. In reverse, the positive value of Zn-doped InSe represents the carrier type is holes. In undoped InSe, the bulk electron density is in the range of 3.35×1014 ~ 3.97×1014 cm-3, and the hall mobility is in the range of 789~1940 cm2/V·s. For the Sn-doped InSe, the bulk electron density increases to 1.47×1016 cm-3. Tin, from the IV group, is the donors for getting the n-type InSe. The mobility of Sn-doped InSe decreases to around 615 cm2/V·s, which is expected and related to the ionized impurity scattering. For the Zn-doped InSe, as acceptors for intrinsic InSe, shows the holes bulk concentration is in the range of 7.85×1013 to 7.98×1013 cm-3. And the mobility of Zn-doped InSe shows the range of 42.8~43.6 cm2/V·s

Parameters	Undoped InSe	Sn-doped InSe	Zn-doped InSe
Sample Thickness (μm)	250	134	404
Content Dopants (%)	N/A	1	3
Current Range (A)	$1.0*10^{-4}$~$7.0*10^{-4}$	$1.0*10^{-4}$~$5.0*10^{-3}$	$1.0*10^{-6}$~$2.0*10^{-5}$
Bulk Concentration (cm^{-3})	$-3.35*10^{14}$~$-3.97*10^{14}$	$-1.47*10^{16}$~$-1.48*10^{16}$	$7.85*10^{13}$~$7.98*10^{13}$
Sheet Concentration (cm^{-2})	$-8.38*10^{12}$~$-9.92*10^{12}$	$-5.94*10^{14}$~$-5.96*10^{14}$	$1.04*10^{12}$~$1.07*10^{12}$
Resistivity (Ω·cm)	8.52~21.7	0.688~0.689	1830~1840
Conductivity ($\Omega^{-1}\cdot cm^{-1}$)	0.0462~0.129	1.45~1.46	$5.42*10^{-4}$~$5.47*10^{-4}$
Hall Mobility ($cm^2V^{-1}s^{-1}$)	789~1940	615~617	42.8~43.6

Table 3.1 the Hall measurement data of undoped, Sn-doped and Zn-doped InSe.

During the measurement, we notice the value of carrier density and mobility keeps change at the different magnitude of the current. By sweeping the magnitude of current, we get the relationship between the carrier density-dependent and the magnitude of the current. At room temperature, the carrier density of undoped InSe presents the decreasing tendency and keep stable at the range of 0.1mA ~ 1mA. Under 0.1mA, the value of the carrier density of undoped InSe keeps stable. For the Sn-doped InSe, the value of carrier density keeps stable from the range of 1μA~10mA. And the Zn-doped InSe, the value of

carrier density, only keeps stable at the range of 1μA ~ 20μA. When the current is greater than 20μA, the carrier density is a positive correlation to the value of current. Combing with the data shown in Table 3.1, Sn-doped InSe shows the smallest resistivity 0.688 Ω·cm, is much smaller than the resistivity of Zn-doped InSe and undoped InSe, 1830~1840 Ω·cm and 8.5~21.7 Ω·cm, respectively. This situation is considered as the value of carrier density dependent on the sample temperature from Joule heating. The resistivity of Zn-doped InSe is much more than Sn-doped InSe and Undoped InSe, as a result, the variation of carrier density of Zn-doped InSe is bigger than the other two samples.

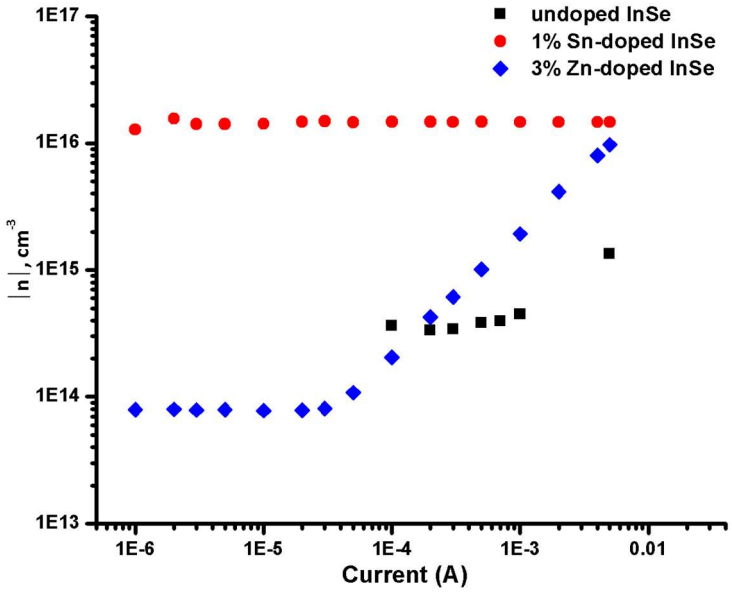


Fig. 3.6 carrier density dependent on the current magnitude

Chapter 4: Characterization of Thin Film InSe FET Devices

4.1 Device Fabrication

Here, we will discuss two types of fabrication processes based on two lithography methods, Photolithography and Electron Beam Photolithography. The content of this sub-section focuses on describe these details of the fabrication process and various methods used in building microscale or nanoscale InSe devices. Other problems solved by this chapter, such as mobility and behavior investigation, are the fundamental parameters to future other applications of InSe in electronics and optoelectronics.

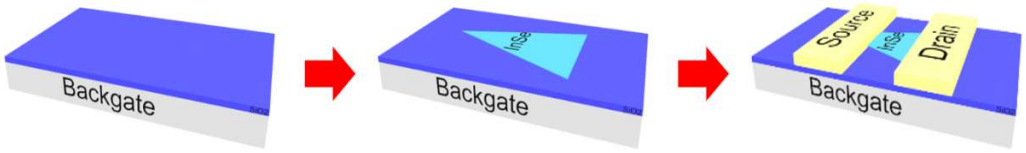
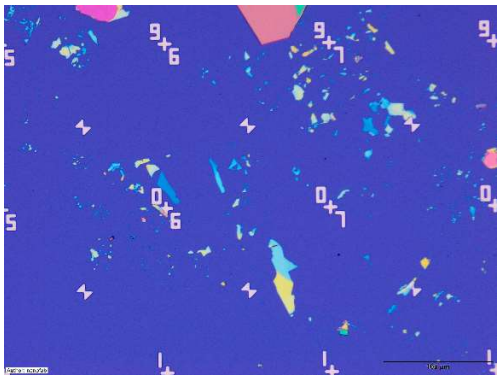


Fig. 4.1 Fabrication process for fabricating InSe field effect transistors. Silicon substrate with 90nm or 300nm Silicon oxide layer be prepared. Pattern and Deposit the gold marker on the surface of silicon oxide. (Not shown). InSe flakes are transferred to the surface of silicon oxide. Find the InSe flakes of targeted thickness under optical microscope and record the marker position. Navigate and locate the position of InSe flakes. Pattern the electrodes area. Deposit the electrodes.

Fig. 4.1 illustrates the fabrication process for building InSe transistors. The fabrication of InSe typically starts with a SiO2/Si substrate with a marker (shown in Fig. 4.2). The thickness of SiO2 is 90nm or 300nm. Then, mechanically exfoliating the InSe flakes with blue tape, and transfer InSe flakes to the SiO2/Si substrate by hotplate (85°C, 2mins). After transferring the flakes, we use the optical microscope to find the thin, smooth flakes

without the bubbles and wrinkle and record the positions of desired flakes. Moreover, coating the LOR 3A/S1813 with the thickness of 200nm/1.5um, navigating the recorded fakes and aligning flakes with the electrodes window of the mask, developing the patterned area and depositing the Ti/Au with the thickness of 10nm/100nm by electron beam lithography. The last process is the lift-off. (shown in Fig. 4.2)

a). b). 

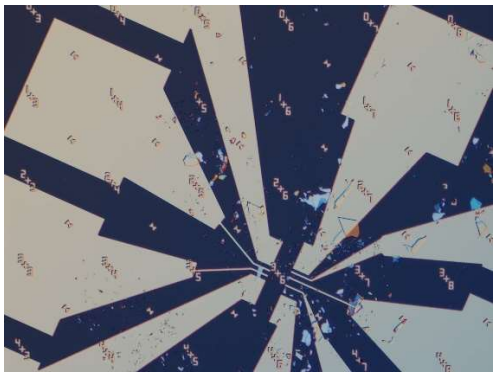
c). d). 

Fig. 4.2 a). the SiO_2/Si substrate with number marker. b). the SiO_2/Si substrate with InSe flakes. c). developed devices and patterned by photolithography. d). deposited devices by Ti/Au.

After lift-off, the process of forming gas annealing is necessary for improving the performance of InSe FET. Several reports have revealed the truth of significant degradation of few-layer InSe in air, which is considered as the chemical reaction with airborne chemicals, such as water or oxygen [7][36]. Forming gas annealing has been applied to

improve the performance of MoS2 FET devices in previous publications [37][38]. Forming gas helps reduce organic residue from the process of mechanical exfoliation and decreases deleterious channel doping without damaging the material [39]. The active ingredient of forming gas is hydrogen gas, which is a good reducing gas to a clear oxide layer. In our process, the InSe FET devices are annealed for 4 hours at 350°C in forming gas. After annealing, the device is cooled down in an argon atmosphere.

The process discussed above is general fabrication steps for our InSe FET devices. Further, to investigate the effect of surface charge doping on the performance of InSe FET devices, we fabricated another two types of devices, one of which is using the PMMA coating layer to protect the materials surface, and the other is encapsulated the InSe flake with h-BN flakes and PMMA coating. Next, I will discuss the fabrication steps of two other devices.

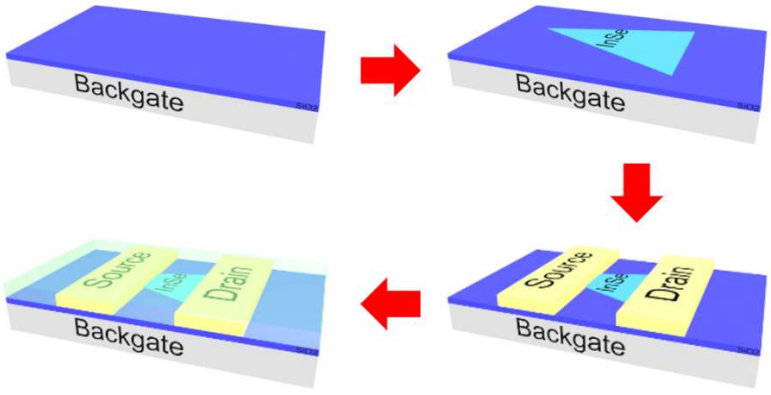


Fig. 4.3. the fabrication process of PMMA-Coated devices.

Devices 4.3 shows the fabrication process of PMMA-coated devices. The procedures of substrates preparation, flakes exfoliation, lithography patterning, metal deposition is the same as previously discussed. After finishing the forming gas annealing, we coated the

PMMA to cover whole devices. The thickness of PMMA layer is 200nm.

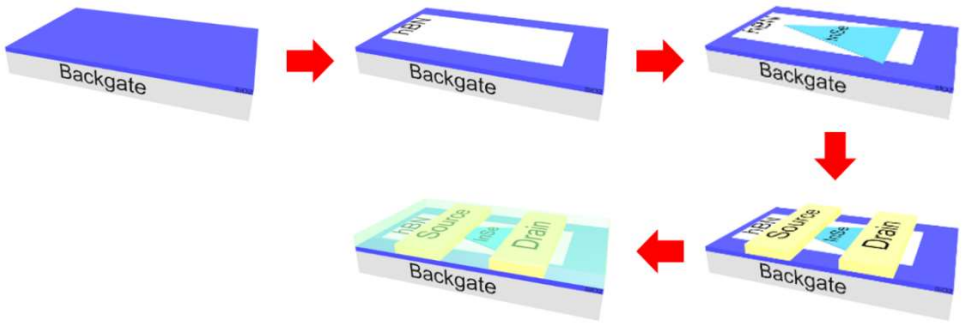
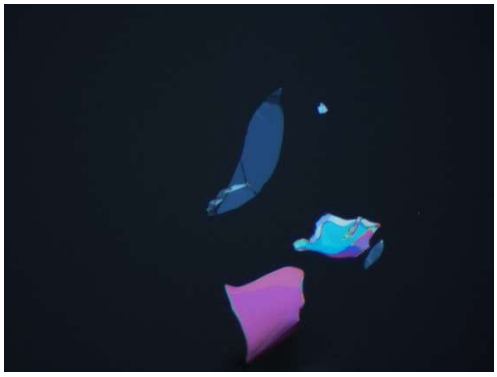


Fig. 4.4 the fabrication process of hBN-InSe-PMMA encapsulated devices

The fabrication process of encapsulated InSe is shown in Fig. 4.4. Firstly, the marked substrate is prepared in the same way previously reported. Using the method of mechanical exfoliation, transfer the hBN flakes to SiO2/Si substrate. Looking for the thin, uniform, large-area, and less organic residue hBN flakes under an optical microscope and recording the position of flakes. Next, preparing the fresh PDMS film and transferring the InSe flakes onto PDMS film. Looking for desired InSe flakes and cutting the area of PDMS with InSe fakes and using the staking station to stack the desired InSe flakes with hBN flakes. Detailed steps include fixing the PDMS film on the glass slide, fixing the SiO2/Si substrate with hBN flakes on the stacking station, finding the hBN flake under the microscope, making the microscope focus on the glass slide and finding the InSe flakes, making the glass slides gradually approaching to substrate, stop when PDMS film and substrate just touched, heating the substrate and making thermal expansion of PDMS, moving away the PDMS film after InSe-hBN staked.

a). b).

c). d). 

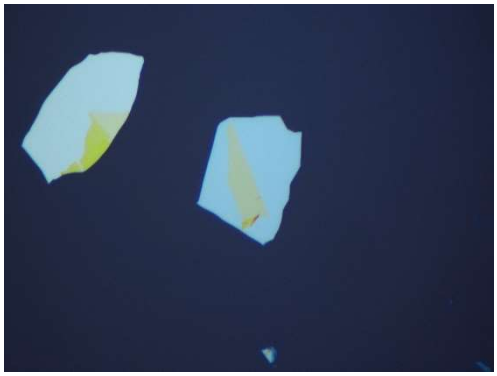
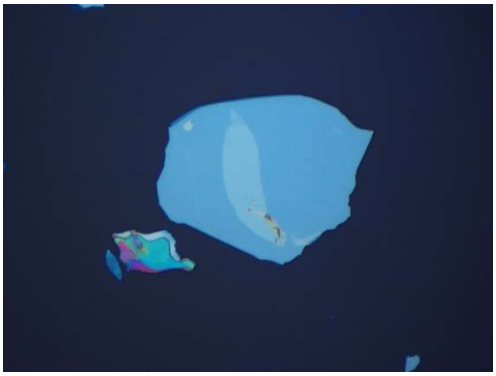
e).  f). 

Fig. 4.5 a) and b) the desired hBN flakes; c) and d) the desired InSe flakes; e) and f) stacked hBN-InSe devices

Then, patterning and deposited the stacked devices. Finally, coating whole devices after forming gas annealing.

4.2 InSe FET Devices Behavior Analysis

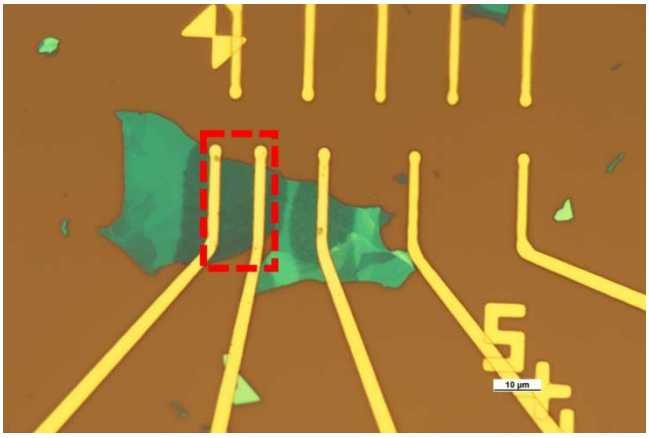
In this subchapter, we would discuss the performance of InSe FET devices. In several

reports, InSe FET devices have already shown mobility of over 103 cm2/V·s [8][40][42]. However, all of them reported many different methods to protect the surface of InSe devices for avoiding performance degradation. In addition, InSe devices are also interested in the topic of quantum confinement effect, which was observed with decreasing thickness of InSe [8][30]. Here, we analyze the effect of surface charge doping on the performance of InSe FET devices and investigate the relationship between layer thickness and device performance. Besides, we will talk about the mobility extraction of InSe FET and the hysteresis phenomenon of InSe FET.

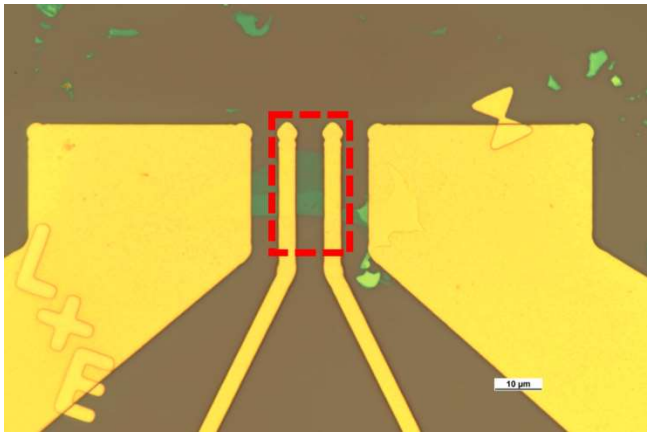
4.2.1 Surface Charge Doping

For Van-der-Waals layered materials, surface charge doping has been shown to have a significant impact on the performance of FET devices. There are many ways to reduce the surface charge doping of 2D materials FET devices, such as PMMA Coating [36][40][43], ALD Al2O3 Deposition [42], Indium-encapsulation [41], hBN-encapsulation [8]. Here, we will compare three types of devices and discuss the effect of surface charge doping on the behavior of InSe FET devices. Firstly, we build the bare InSe devices without any coating layer. Secondly, we build the PMMA coated devices. Finally, we build the hBN-PMMA encapsulated devices. Here is the optical image of three types of devices, shown in Fig. 4.6.

a).



b).



c).

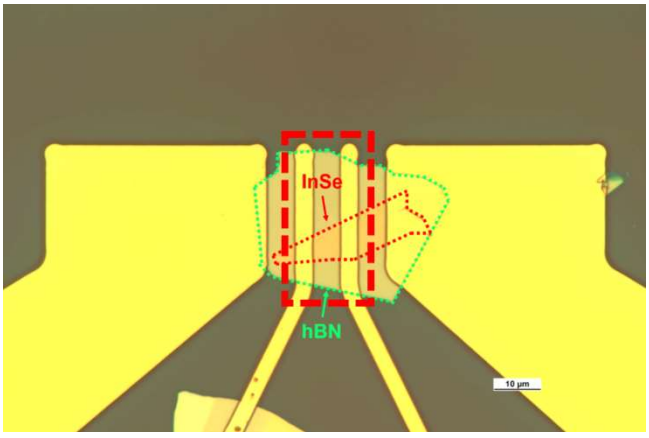
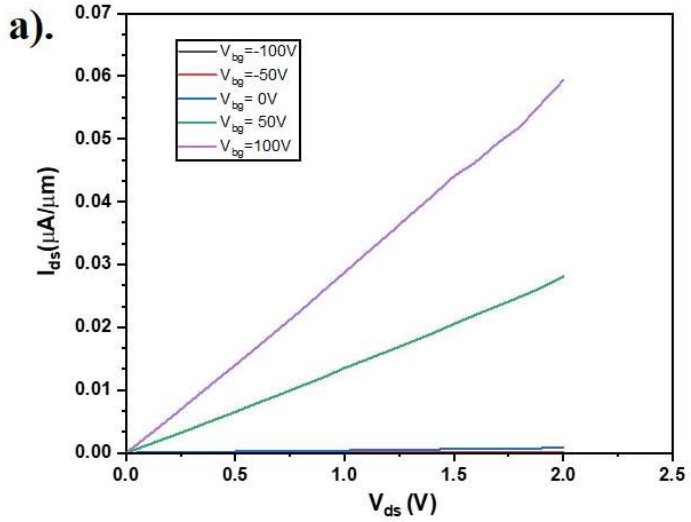
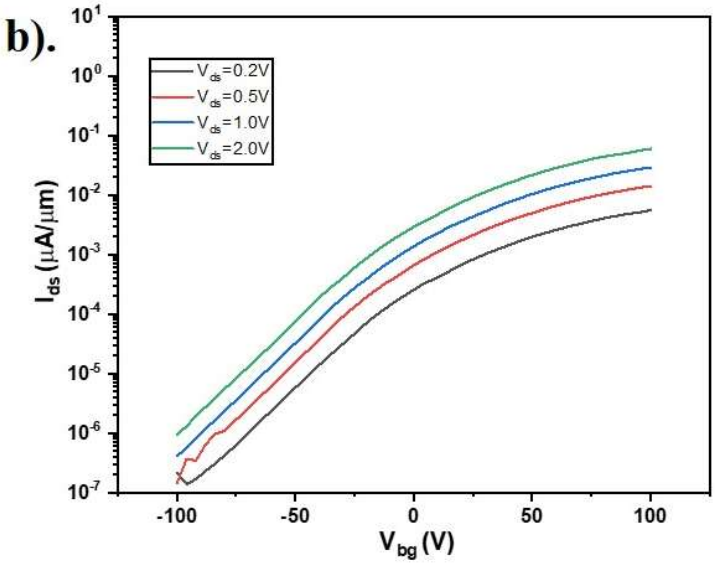


Fig. 4.6 Three types of FET device for analyzing surface charge doping. a). Bare device, the measured device marked by the red dotted box. b). PMMA Coated device, the measured device marked by the red dotted box. c). hBN-PMMA encapsulated device, the green box is hBN, the small dotted box is InSe flake, the big dotted box is the measured device.

Indium Selenide has been proven to be very unstable in the air because of the effect of H2O and O2 molecules [36][42]. Firstly, the O2/H2O be regarded as a p-type dopant due to negative redox potential [44]. In theoretical calculation, the Se vacancy could be passivated by oxygen leading to the formation of trap states [46].





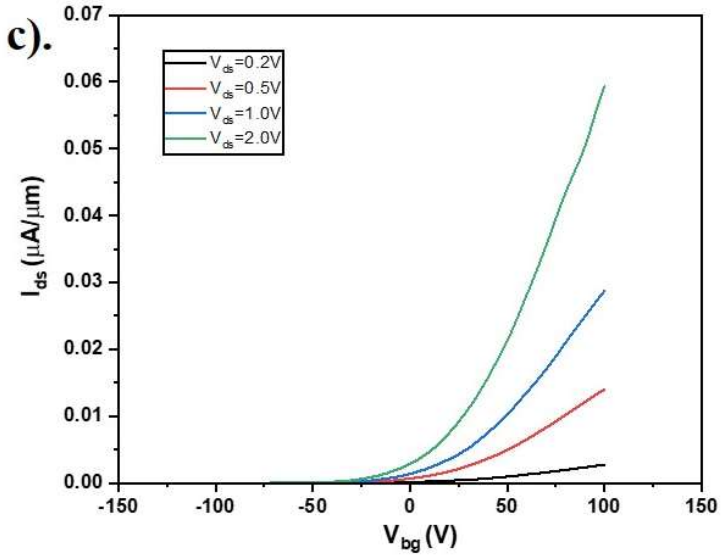
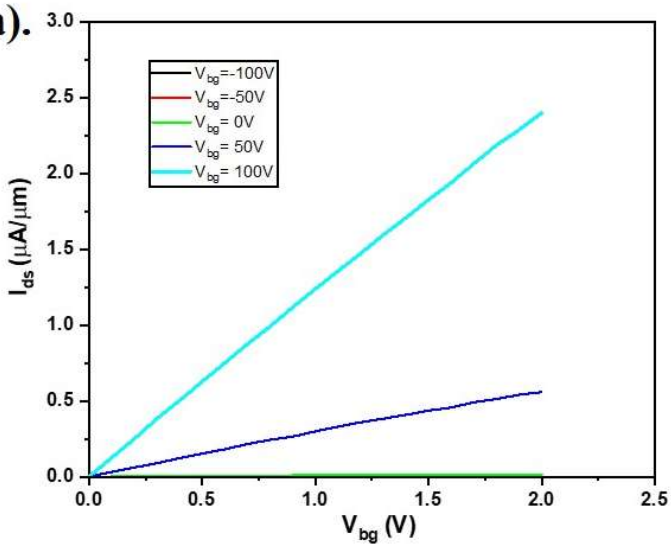


Fig. 4.7 a). I-V curve of bare InSe FET devices applied by back gate Voltage, the V_{bg} sweeping from -100V to 100V, the step is 50V. b). transfer curve of bare InSe FET devices in log scale, V_{ds} = 0.2V, 0.5V, 1.0V, 2.0V, respectively. c). transfer curve of bare InSe in normal scale

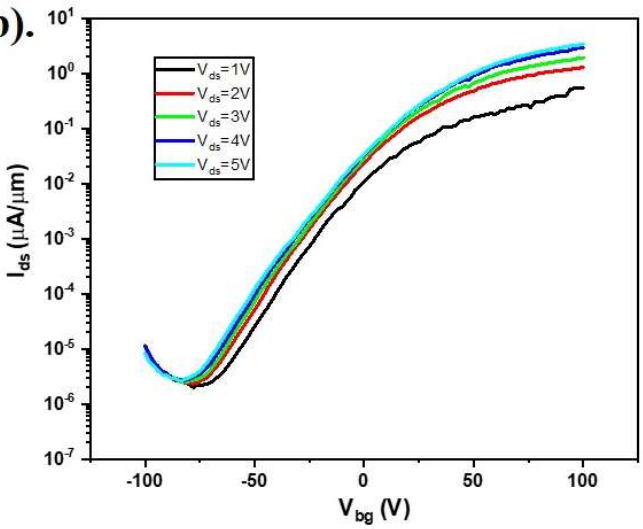
From Fig. 4.7, we observed that the FET devices could not be completely turned off at Vds = 2V, even the Vbg = -100V. And the threshold voltage keeps shifting when sweeping the drain-source voltage. These results are considered surface doping when measuring the devices in air condition.

For investigating the effect of surface charge doping, we coated the devices with polymethyl methacrylate (PMMA) after annealing. PMMA has been proven to improve the FET performance in previous articles [30][36]. Firstly, PMMA is a good dielectric material, which helps to improve the FET mobility of devices. Secondly, PMMA helps to screen the Coulomb potential from trapped charges in the substrate, which causes the performance reduction of FET devices.

a).


V_{bg}=-100V
V_{bg}=-50V
V_{bg}= 0V
V_{bg}= 50V
V_{bg}= 100V
I_{ds} (μA/μm)
V_{bg} (V)

b).


V_{ds}=1V
V_{ds}=2V
V_{ds}=3V
V_{ds}=4V
V_{ds}=5V
I_{ds} (μA/μm)
V_{bg} (V)

c).

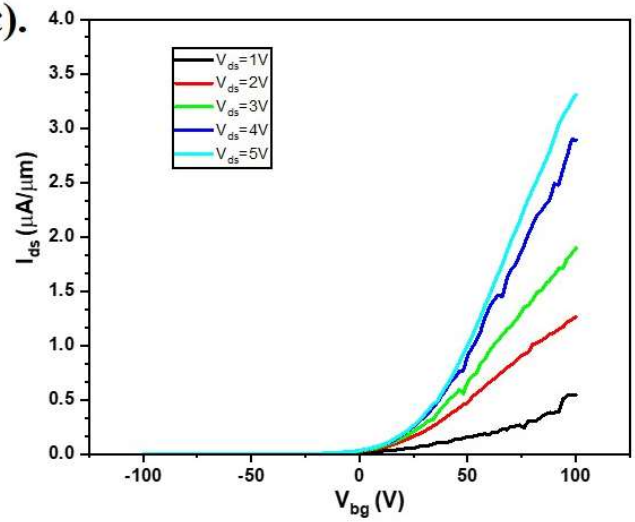

V_{ds}=1V
V_{ds}=2V
V_{ds}=3V
V_{ds}=4V
V_{ds}=5V
I_{ds} (μA/μm)
V_{bg} (V)

Fig. 4.8 a). I-V curve of PMMA Coated InSe FET devices applied by back gate Voltage, the Vbg sweeping from -100V to 100V, the step is 50V. b). transfer curve of bare InSe FET devices in log scale, Vds = 1.0V, 2.0V, 3.0V, 4.0V, 5.0, respectively. c). transfer curve of bare InSe in normal scale

In Fig. 4.8, we observed the PMMA coated InSe keep the same threshold voltage when drain-source voltage sweeping from 0.5V to 5.0V. In the log-scale graph, the off-current of FET also keeps the same value when drain-source voltage sweeping from 0.5V to 5.0V. We concluded that the PMMA coating layer improves the stability of InSe FET devices, which screen the charge doping of materials surface.

To further investigate the effect of surface charge doping, we fabricate the hBN-InSe-PMMA encapsulated devices. Hexagonal boron nitride is a typical 2D insulator material because of the large bandgap, 5.2 eV. And hBN thin flakes also provide atomic-scale flat surface for InSe FET devices.

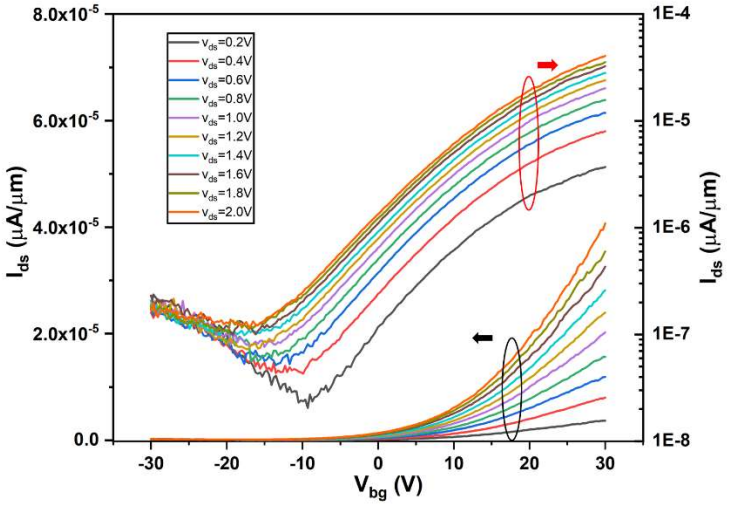


Fig. 4.9 Transfer curve of hBN-InSe-PMMA encapsulated devices

In Fig. 4.9, the off current of the FET device is decreasing with the reduction of the drain-source voltage. And the threshold voltage keeps the same value when the drain-source voltage is sweeping. The hBN thin layer helps back gate providing better controllability than silicon oxide comparing with Fig. 4.7, and Fig. 4.8.

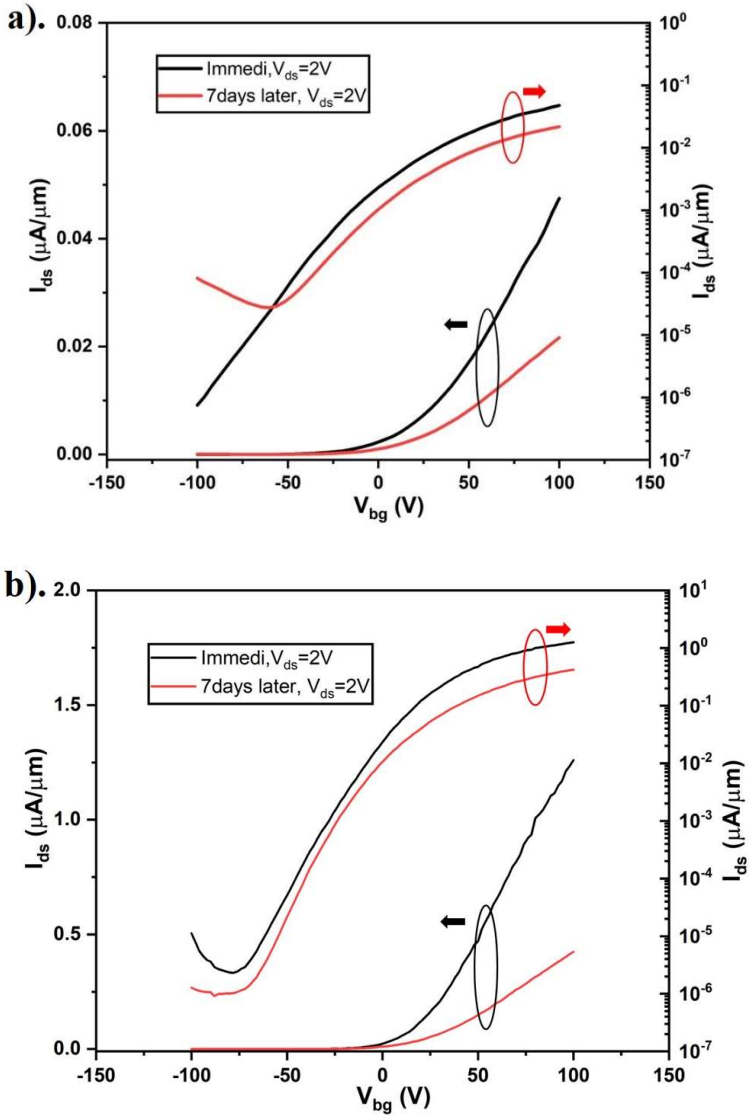


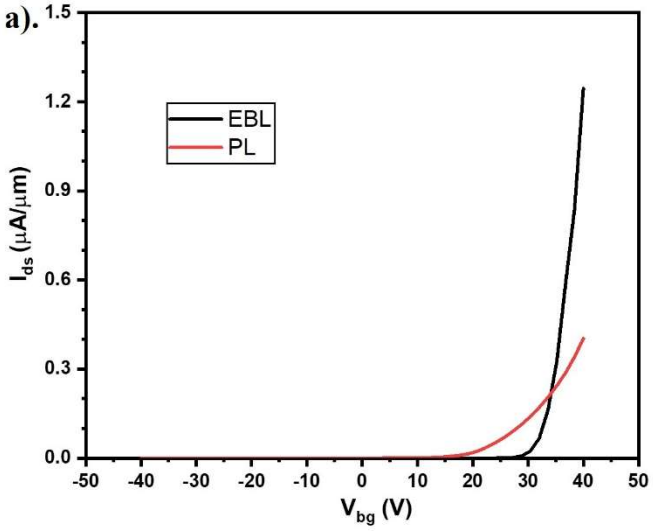
Fig. 4.10 a). Comparison of transfer curve of bare InSe FET in immediate day and 7 days later. b). Comparison of transfer curve of PMMA coated InSe FET in immediate day and 7 days later.

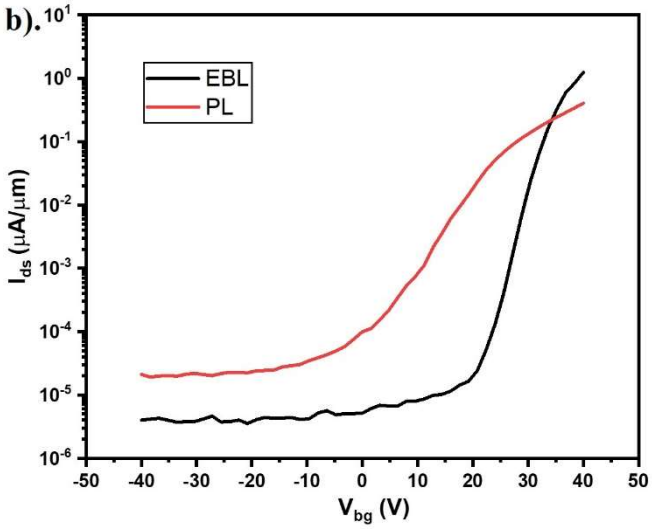
The behavior of the bare device presented the ambipolar behavior after explored in air condition, as shown in Fig. 4.10 a. It means the InSe channel to be doped by the holes, which provided by oxygen in the air. On the other side, the PMMA coated devices keep the same n-type behavior after 7 days later, which means the PMMA coating layer isolates the doping effect in air condition.

In summary, the PMMA coating layer helps devices to resist the doping effect of air condition, which improve the stability of devices. As a good dielectric material, the PMMA coating layer also screens the Coulomb potential from trapped charges on the channel surface.

4.2.2 Fabrication Process Influence on FET performance

We apply two type lithography methods to fabricating back gate InSe FET, Electron Beam Lithography (EBL) and Photolithography (PL). The fabrication steps are the same for both methods, including mechanically exfoliation, flakes location, photoresist coating, patterning, developing, metal deposition, lift-off and annealing, in order. The same distance of channel length with 5um was defined. The same thickness (10/90nm) and materials (Ti/Au) of contact metal was deposited. The dielectric layer is 90 nm SiO2. The only difference comes from the types of photoresist. The photoresist of Photolithography is LOR 3A and S1813 with the thickness of 200nm/1.5um. For the Electron beam lithography, the photoresist is PMMA with thickness of 260nm.We found the EBL device shows better performance than PL device, in the on/off ratio, subthreshold swing, on-status current and mobility.


a).
EBL
PL
I_{ds} (μA/μm)
V_{bg} (V)


b).
EBL
PL
I_{ds} (μA/μm)
V_{bg} (V)

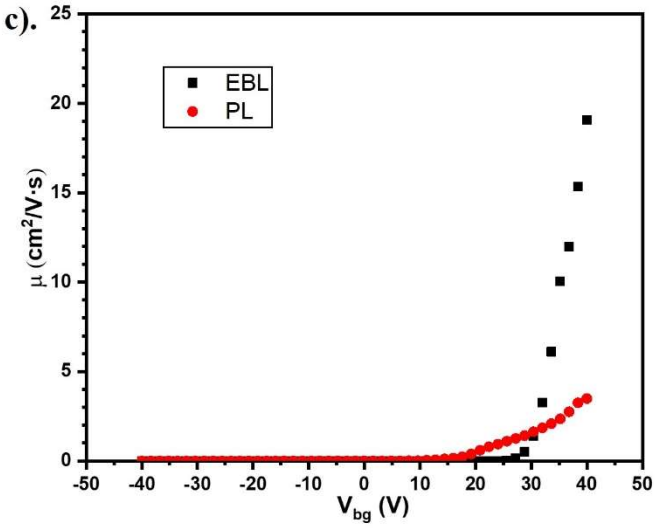

c).
EBL
PL
μ (cm²/V·s)
V_{bg} (V)

Fig. 4.11 a). Transfer curve of InSe FET d fabricated by E-beam Lithography and Photolithography, respectively. V_{ds}=2V, in normal scale. b). Transfer curve of InSe FET fabricated by E-beam Lithography and Photolithography, respectively. V_{ds}=2V, in log scale c). Field Effect mobility of InSe FET fabricated by E-beam Lithography and Photolithography, respectively.

As shown in the figure 4.8, both of EBL device and PL device were measured under the vacuum situation to avoid the influence of surface charge doping. At figure 4.8 a) and b), the on-status current of EBL device is higher than PL device because of the contact resistance reduction in EBL device. Moreover, the subthreshold swing of EBL device is around 1.4V/decade, smaller than its of PL device, 6.4V/decade. It was expected as the less residue of photoresist between the contact metal and InSe, which reduced the trapped charge at the interface and helped to get smaller subthreshold swing. Also benefiting from less trapped charge at interface, the off-current of EBL device is smaller than its of PL device. Because the trapped charge of photoresist provided extra current channel at the interface between contact metal and InSe when FET was turned off.

4.2.3 Extraction of key parameters in InSe FET

The key parameters of FET include the on-off ratio, threshold voltage, and mobility. In our two-terminal FET devices, the field-effect mobility μFE is extracted from the transconductance:

$$g_m = \frac{I_{ds}}{V_{gs}}$$

The two-terminal field effect mobility was calculated from the formula:

$$\mu_{FE} = \frac{L}{W} \cdot \frac{g_m}{C_i V_{ds}}$$

In the formula, where L and W are the length and width of the channel, Ci is the capacitance per unit area of the dielectric layer (Ci = ε0εr/d, ε0 is free space permittivity, εr is the dielectric constant of insulator layer and d is the thickness of insulator layer). For 300nm SiO2 substrate, the Ci = 11.6 nF/cm2.

Parameter	Device 1	Device 2	Device 3	Device 4
Fabrication Process	Photolithography Bare	Photolithography PMMA Coating	Photolithography Bare	EBL Bare
Dielectric layer thickness (nm)	285	285	90	90
μ_{FE} ($cm^2/V \cdot s$)	0.3	6	3.5	20
I_{on}/I_{off}	10^4	10^6	10^4	10^5
I_{on} ($\mu A/\mu m$)V_{ds}=2V	0.06	1.4	0.4	1.25
Subthreshold Swing (V/decade)	20	12.5	6.4	1.4
Testing Condition	Air	Air	Vacuum	Vacuum

Table 4.1 Key parameters of InSe FET devices

We collected three sets of devices in three different structures, including three bare devices, 7 PMMA-Coating devices, and 1 PMMA-hBN encapsulated device. By comparing the calculated results of bare devices and PMMA-Coating devices, we found the PMMA-Coating devices present higher mobility value, higher on-current, and higher on/off ratio, which attributed to the effect of trapped charge screening and isolating the surface charge doping from PMMA coating layer.

4.2.4 Thickness Dependency

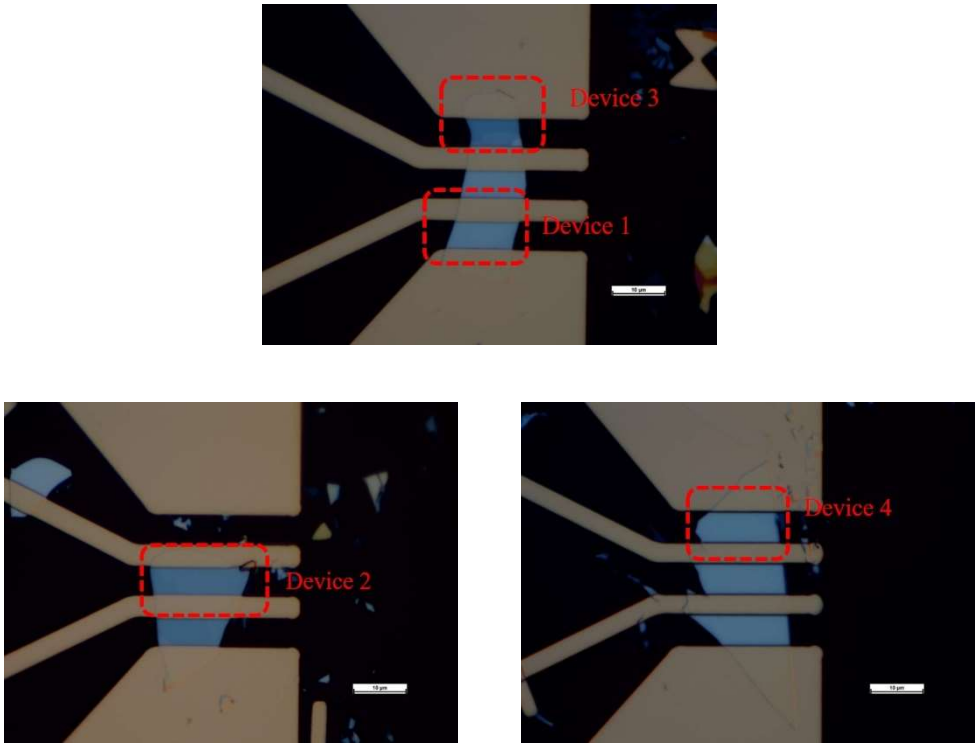


Fig. 4.12 Two terminal FET devices with different thickness flakes

Thickness dependent transport characteristics of Van-der-Waals materials have been investigated for many researchers. Li et al. and Das et al. conclude that Coulomb scattering from charged impurities and resistor network both contribute to the thickness-dependent transport property [50][51]. Especially for the back-gate FET devices, the depletion region is formed at the bottom position of flake. The distance between top contact and the depletion region depends on the flake thickness. When thickness decreasing, the current flow will be more easily controlled by back-gate. In our experiment, we make four FET devices with different thickness flakes, as shown in Fig. 4.11. Combing with color-thickness dependency of InSe flakes, we identify the devices 3 has the thinnest flake. By comparing the transfer curve of four devices, we conclude that the on/off ratio is highly dependent on flakes thickness. The device 3 shows the best on/off ration from four devices.

Although devices 1 shows the highest current density, the gate could not turn off the device.

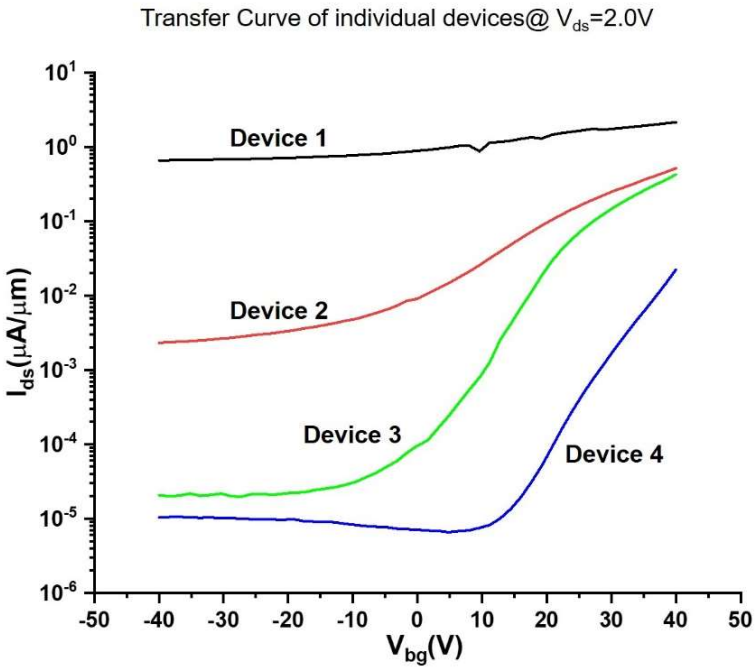


Fig. 4.13 Transfer curve of FET devices at different thickness

	Mobility	I_{on}/I_{off} @V_{ds}=2V	V_{th}
Device 1	-	-	-
Device 2	2.3 $cm^2/V·s$	2×10^2	20.6V
Device 3	2.5 $cm^2/V·s$	2×10^4	22.3-24.4V
Device 4	0.304 $cm^2/V·s$	3.5×10^3	31.3-35.3V

Table 4.2 the key parameters of 4 FET devices with different thickness

4.2.5 Hysteresis Loop

In many studies of Van-der-Waals materials FET devices, the hysteretic behaviors in conductance characteristics are investigated for many times. The hysteresis, defined as the magnitude of the threshold voltage shift, depends significantly on gate bias sweeping rate [70]. And the hysteresis is mainly dependent on the trapped charges between the 2D channel materials and the surface of SiO_2. The annealing was found to suppress the

hysteresis effectively [54].

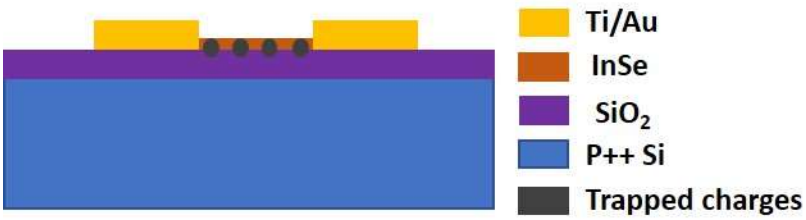


Fig. 4.14 Mechanism of hysteresis for InSe backgate FET, the trapped charges includes the Si-OH silanol groups and water molecules

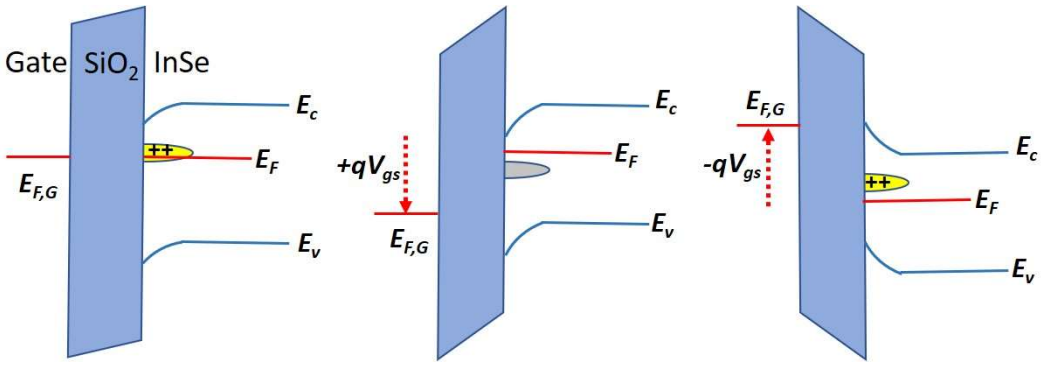


Fig. 4.15 Band diagram of the InSe/SiO2/Si structure (Si is treated as degenerate), at zero (a), positive (b) and negative (c) gate bias, showing that a negative Vgs favors the storage of positive charge at the InSe/SiO2 interface.

By introducing the hysteresis width and trapped charge formula, we could calculate the hysteresis loop and trapped charges in the form of quantity.

Hysteresis Width[81]:

$$W = |V_{gs1}(I_w) - V_{gs2}\ (I_w)|$$

Trapped Charge[81]:

$$n_t = \mathrm{W} \cdot \frac{C_{ox}}{|q|}$$

Most earlier reports have talked the large variations in hysteresis of MoS2 FET, which caused by extrinsic/environmental effects. And they also proposed annealing and encapsulation would reduce the hysteresis loop and even eliminate hysteresis [70][71]. Based on previous work and experience on MoS2, we have applied the forming gas annealing to multilayer InSe FET. However, considering the back-gate FET structure of our devices, we need to further reduce the hysteresis. Thus, we switch the dielectric layer from 285nm SiO2 to 90nm SiO2, even to 50nm SiO2

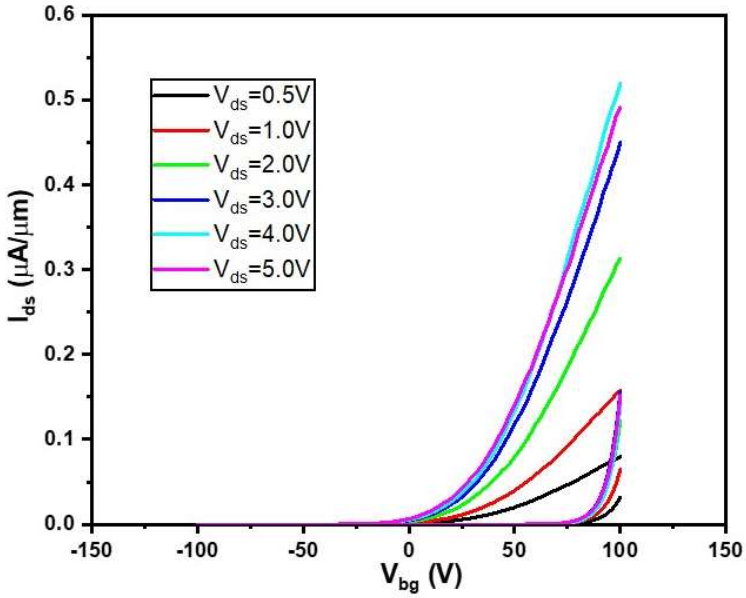


Fig 4.14 the typical hysteresis transfer curve of InSe FET on 300nm SiO_2 substrate.

In our experiments, we start from the 300nm SiO2, the typical hysteresis loop shown in Fig. 4.14. When Vbg sweeping from 100V to -100V and back to 100V, the change of gate bias sweeping direction from backward to forward induced a noticeable negative threshold voltage shift up to ~50V and improved drain-source current. Hysteretic behavior has been observed in a variety of typical other 2D materials devices, like MoS2 FET [54]. Charge injection at the interfaces between semiconductor and substrate and charge transfer from neighboring adsorbates have been attributed as two possible factors in charge trapping

and thus the resultant hysteresis, considering the thermally grown silicon oxide has effective trap densities Nit ~ 5×1010 cm-2 and Nit ~ 5×1011 cm-2 [55].

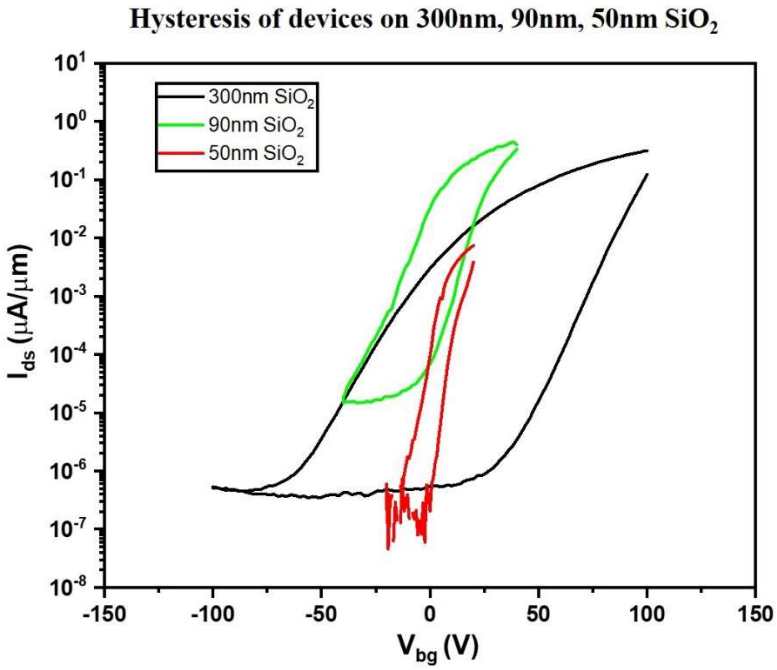


Fig 4.15 the hysteresis loop comparison of InSe FET on the dielectric layer of 300nm SiO_2, 90nm SiO_2 and 50nm SiO_2

When switching the dielectric layer to thinner one, the capacitance of dielectric layer will be improved. The back-gate voltage injects more electrons into the channel. It means that more carriers are provided for the electron transportation of channel. Thus, the control ability of back gate is enhanced. On the other hand, because same thickness InSe has the same ability to trap charge from ambient environment, when induced more carrier, the electron transportation of channel is less affected by the trapping charge. As a result, the hysteresis loop is reduced by the decreased thickness of dielectric layer.

Chapter 5: Summary & Future Works

5.1 Summaries

In this thesis, we have addressed several key issues that are critical for the future research of InSe in electronic and optoelectronic systems.

First, the growth of ε-polytype InSe, Sn-doped InSe (n-type) and Zn-doped InSe (p-type), characterized by TEM, XRD and Raman. we have grown the ε-polytype InSe. We doped the intrinsic InSe single crystal by Tin and Zinc substance to get n-type InSe and p-type InSe. We also investigated the βcrystal structure parameters, energy bandgap and bond type by XRD spectrum, PL spectrum and Raman spectrum. Further, we observed the atom distribution and the image of crystal structure by TEM.

Second, Measuring the Hall effect mobility and carrier density of undoped InSe, Sn-doped InSe and Zn-doped InSe. In order to understand the electrical characteristics of InSe and application potential in the semiconductor filed, we analyzed the electrical properties of InSe in bulk form by using Hall Effect Measurement System. We got the measurement results including conductivity, resistivity, carrier type, carrier concentration and Hall Effect mobility.

Third, investing the relationship between Transistor performance parameters (including on/off ratio, on-status current level, field effect mobility, subthreshold swing and threshold voltage) and Fabrication process (Coating layer, lithography method). As Van-der Waals layered materials, the research of carrier transportation in thin film InSe is a very important part of this thesis. The main research interests include the fabrication process of multilayer InSe FET, the performance of multilayer InSe FET, the optimization

of InSe FET and the Field Effect mobility of thin film InSe. In detailed, we used both Electron Beam Lithography and Photolithography to fabricate InSe FET. The photoresist used in different lithography methods will affect the interface between the contact metals and InSe and also have an influence on the on/off ratio, subthreshold swing and on-status current of FET. Next, we applied the PMMA as a coating layer for suppressing the trapped charge by InSe. The PMMA file is hydrophobic dielectrics, which is conducive to improving interface conditions by suppressing carrier scattering from chemical impurities. Then, we built different thickness InSe FETs to investigate the thickness dependency of FET performance. We found the thicker InSe FET have higher current level than thinner one, but the on/off ratio will decrease with the increase of thickness.

Last, investigating the relationship between hysteresis behavior of FET and dielectric layer thicknesswe talked about the hysteresis in InSe FET. The mechanism of hysteresis is dominated by the trapped charges between the interface between channel materials and SiO_2. And the width of hysteresis loop is related to the dielectric constant. In our experiments, instead of changing dielectric layer, we reduced the thickness of SiO_2. By the way, we reduce the range of backgate voltage to switch the transistor. Because of the smaller sweeping range, the less trapped charge will be attracted and fixed at the surface of SiO_2, which helps to reduce the hysteresis loop in our FET.

5.2 Future Works

To deeply understanding the transport properties of InSe, there are more future works need to be done. For the bulk form, the low-temperature Hall Effect Measurement need to be done, which helps to get the relationship between the Hall Mobility vs temperature

dependency. The hall mobility is affected by temperature because the phonon scattering is large dependent on the temperature. To investigate the low temperature Hall Effect Mobility, we would deeply understand the mechanism of electron transportation of Van der Waals layered materials.

For the thin flakes form, improving the mobility of InSe FET is the first work to be done. There are many very effective methods could improve the mobility of InSe FET, including use High-K dielectric materials (Al2O3, HfO2), using four probe configurations to eliminate the influence of contact resistance.

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