5GHz Doherty Amplifier Designed in Triquent GaAs Process

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Abstract of Thesis

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Modern communication systems are incorporating spectrally efficient modulation schemes in an attempt to get closer to the maximum transmission data rate. These modulation schemes tend to be a combination of amplitude and phase modulation schemes and require extremely linear transmitters. The bottleneck in most modern transmitters is the power amplifier. The linearity and power efficiency of the power amplifier determines the quality of the transmitter to a large degree. Generally, power amplifiers are either very efficient and very non-linear or very linear with moderate to low efficiency. Thus transmitters which require high linearity usually operate the power amplifier below the maximum efficiency point and have a narrow input power range over which the amplifier is linear.

Recently, designers are using an old structure which solves the problem of linearity and efficiency simultaneously. The Doherty Amplifier structure is being investigated at higher frequency ranges and higher output power. Up to this point, Doherty structures at frequencies of 2 to 2.5 GHz have been reported in literature. Most of structures were not fully integrated on chip. The input matching circuit and output power combiners were manufactured at the board

level. This thesis shows a Doherty structure at an extended frequency range with all of the components on chip. The commercial GaAs process from Triquent was used in the implementation. The simulated results along with measured results are presented.

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List of Acronyms

AM	Amplitude Modulation
D-Mode	Depletion Mode
E-Mode	Enhancement Mode
GaAs	Gallium Arsenide
G-S-G	Ground Signal Ground
MIM	Metal Insulator Metal
OFDM	Orthogonal Frequency Division Multiplexing
OPBO	Out Put Back Off
PAE	Power Added Efficiency
pHEMT	Pseudomorphic High Electron Mobility Transistor
PM	Phase Modulation
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
S-Parameter	Scattering Parameter

Chapter 1: Introduction

1.1 Motivation and Background

Communication systems are designed to send information from a source that generates the information to one or more destinations. A block diagram of a communication system is represented below. The heart of the communication system consists of three parts, the transmitter, the channel, and the receiver. The transmitter converts the electrical signal into a form that is suitable for transmission through a suitable medium. The transmitter performs the matching of the information signal to the medium by a process called modulation. Modulation changes the sinusoidal carrier signal by systematically varying the carrier's amplitude, frequency or phase. The choice of the type of modulation is based on several factors, such as the amount of bandwidth allocated, the types of noise and interference that the signals encounter, and the electronic devices that are available for signal amplification prior to transmission. Amplitude modulation is a means of transmitting information by changing the amplitude of the carrier signal. The amount by which the carrier signal amplitude is varied corresponds to the low frequency information to be transmitted. Frequency modulation is a means of transmitting information by

changing the frequency of the carrier signal. The amount by which the carrier signal's frequency is changed corresponds to the low frequency data to be transmitted. Phase modulation is a means of transmitting information by changing the phase of the carrier signal. Similarly, the amount by which the carrier signals' phase changes corresponds to the low frequency data to be transmitted. Most modern communications systems incorporate a combination of the above mentioned modulation schemes. Quadrature Amplitude Modulation is a combination of digital amplitude and digital phase modulation. [1] In this modulation scheme, the amplitude and phase can have discrete values. The result of this modulation scheme is an output signal that is analogous to an M-bit word. In Quadrature Amplitude Modulation schemes, the reliability of the transmitted data depends on the linearity of the amplitude modulation scheme and the linearity of the phase modulation portion for the various discrete levels.[2] Large non linearity can cause the discrete amplitude and phase changes to be indistinguishable thus making the reception of the low frequency data very hard. The Power Amplifier is the last active device in the transmitter chain. The power amplifier can be characterized in terms of its linearity and efficiency [3]. The power amplifiers job is to increase the power applied at its input by a fixed amount. It is also desirable to maintain a constant phase relationship between successive input pulses over all input power levels.

Unfortunately, this does not happen. The ratio of output power to input power decreases as the input power increases and the phase relationship between the input and output signals also changes as a function of the input power levels. For Quadrature Amplitude Modulation based schemes, these power amplifier errors can cause severe transmission errors that make the receiver design very difficult.

1.2 Statement of Research

High efficiency and good gain linearity are both required for modern communications such as M-ary QAM or OFDM schemes [1]. For Solid State Power Amplifiers, good linearity response requires operation at an input power level that is backed off several dB from the point where the output power saturates. Unfortunately, this Output Power Back Off point does not yield optimal power efficiency. The Doherty Amplifier was introduced in the 1930's as new form of linear amplifier [4]. W. H. Doherty implemented this scheme using external components and vacuum tube amplifiers. Most recently, the Doherty amplifier has had resurgence at the 1 to 2 GHz range [5] [6] [7]. The highest operation frequency for Doherty Amplifiers reported in recent journals is 2.3 GHz. The amplifier is usually implemented with discrete transistors and the Wilkinson power divider, attenuator, input matching network and output

power combining network are implemented off chip. Our Goal in this work is to realize the Doherty Amplifier at an operating frequency of 5 GHz with the discrete transistors and the Wilkinson power divider, attenuator, input matching network and output power combining circuits implemented on chip.

1.3 Overview of Dissertation

Chapter II contains a detailed summary of the literature review. Non-linear effects in power amplifiers will be covered. The modeling and extraction of these non-linear effects will be discussed. AM-AM and AM-PM effects along with its impact on communication systems will be discussed. Efficiency enhancement and linearity enhancement techniques for power amplifiers will also be covered. The enhancement technique discussion illustrates the usefulness of the Doherty Amplifier technique. The literature review section will end with a basic review of Class A and Class C power amplifier design. Chapter III is the methods section. In this section, the Doherty Amplifier is reviewed in more detail. A simple model will be used to explain the load modulation concept which is the core principle of operation for the Doherty Amp. Next, a short review of the methods used to determine optimum device sizing and load impedance will be discussed. Finally, derivations and calculations will be presented for the remaining blocks that make up the

Doherty configuration. These blocks include a Wilkinson power splitter, an Attenuator, a Class A Power Amp, a Class C Power Amp, and the Output Combining Network for the entire configuration. Chapter IV is the implementation section. Circuit schematics and layouts are presented in this section. Pre-layout and post layout simulations including S-parameter, Power Efficiency, and Two-tone Intermodulation simulations are presented. Measured data is also presented in this section and compared to simulation results. Chapter V is the conclusion. A summary of the work is presented and recommendations for future research are proposed including ideas for pre-distortion and a K-band implementation.

Chapter 2: Literature Review

In this chapter, we will try to summarize some of the important properties of Power Amplifiers. These properties are important for the design of power amplifiers as will be shown in the following chapter. We will introduce the source of nonlinearity's in power amplifiers as well as the amplifiers AM-AM and AM-PM effects. The efficiency of the amplifier will be defined and formalized. The relevant literatures to the topics discussed will be listed.

2.1 Non-Linear Effects in Power Amplifiers

The Taylor series expansion can be used to express the drain current of a transistor as a function of the input voltage "*v*" [8].The Taylor series is expanded around a bias voltage "V_0".

$$i_D = f(v) \tag{2.1}$$

$$f(v) = f(V_0) + \sum_{n=1}^{\infty} \frac{1}{n!} \frac{\partial^n f(v)}{\partial v^n} (v - V_0)^n \tag{2.2}$$

The non-linear behavior of the transistor can be determined by the two tone excitation test with signal components separated by small frequencies. Assume the input voltage for the transistor takes the following form:

$$v = V_0 + V_1 cos\omega_1 t + V_2 cos\omega_2 t \qquad (2.3)$$

$V_0 = DC\ voltage\ applied$
$V_1 = amplitude\ of\ the\ sinusoid\ @\ \omega_1$
$V_2 = amplitude\ of\ the\ sinusoid\ @\ \omega_2$

The drain current can be expressed using the first three derivatives of the Taylor series expansion and equation (2.1). By collecting all frequency component terms, certain conclusions can be made about the results.

$$\begin{aligned} i_D = {} & f(V_0) + \frac{1}{4}\frac{\partial^2 f(v)}{\partial v^2}(V_1^2 + V_2^2) + \left[f'(V_0) + \frac{1}{4}\frac{\partial^3 f(v)}{\partial v^3}\left(\frac{1}{2}V_1^2 + V_2^2\right)\right] V_1 cos\omega_1 t \\ & + \left[f'(V_0) + \frac{1}{4}\frac{\partial^3 f(v)}{\partial v^3}\left(\frac{1}{2}V_2^2 + V_1^2\right)\right] V_2 cos\omega_2 t \\ & + \frac{1}{4}\frac{\partial^2 f(v)}{\partial v^2}(V_1^2 cos2\omega_1 t + V_2^2 cos2\omega_2 t) \\ & + \frac{1}{24}\frac{\partial^3 f(v)}{\partial v^3}(V_1^3 cos3\omega_1 t + V_2^3 cos3\omega_2 t) \\ & + \frac{1}{2}\frac{\partial^2 f(v)}{\partial v^2} V_1 V_2 \cos(\omega_1 \pm \omega_2)\, t + \frac{1}{8}\frac{\partial^3 f(v)}{\partial v^3}[V_1^2 V_2 \cos(2\omega_1 \pm \omega_2)\, t \\ & + V_1 V_2^2 \cos(\omega_1 \pm 2\omega_2)\, t] \end{aligned} \qquad (2.4)$$

First, the even harmonic components are a result of the even order derivatives and the odd harmonic components are a result of the odd order derivatives. Second, the first order mixing terms "$\omega_1 \pm \omega_2$" are dependent on the even order derivatives. The first order mixing terms fall out of the frequency band of interest and contribute little to the overall distortion of the device. The mixing

products of the third and higher orders are mainly determined by the odd derivatives of the device transfer function. These terms fall into the frequency band of interest and contribute significantly to the overall distortion of the device. The frequency band of interest is the carrier frequency plus or minus the frequency of the baseband data which has been up converted. The analysis above assumes to separate carriers with fixed spacing. In practice, such a signal will be the result of the amplitude modulation of a single carrier. The two-carrier signal would be the resultant spectrum from a double sideband suppressed carrier AM system with a single, fixed frequency, modulating tone [9]. The spectrum resulting from non-linear amplification has a stepped appearance as shown in figure 2, with each step corresponding to a higher order of distortion. The spectral region of most concern in a regulated communications band is the third order step, which is the one that lies closest to the main signal. The third order step is known as the adjacent channel and the main specification associated with it is the integrated power which lies in this channel. This power is commonly known as the Adjacent Channel Power [10].

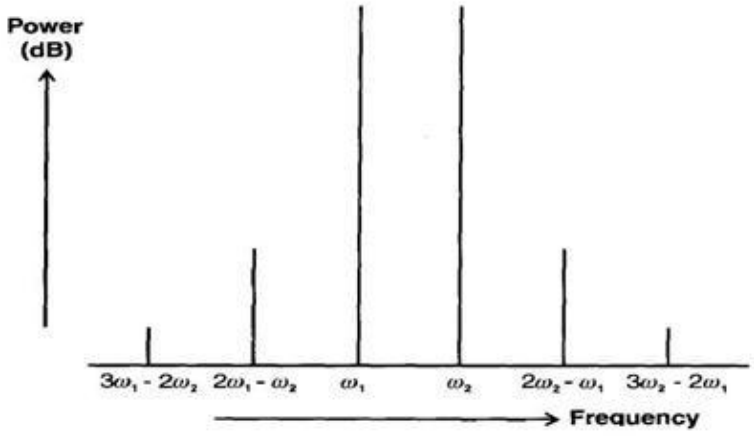

Figure 2.1-Intermodulation Spectrum [11]

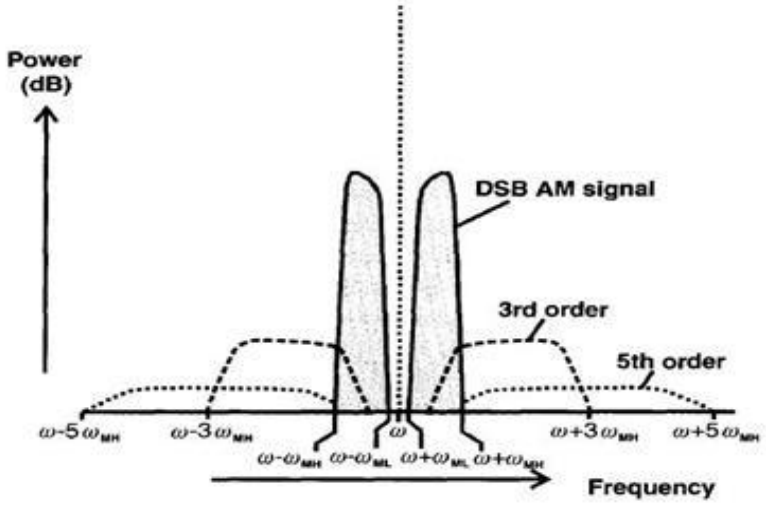

Figure 2.2-Analog Amplitude modulation spectrum [10]

2.2 Definitions of AM-AM and AM-PM Effects

2.2.1 AM-AM Effects

Power Amplifier distortion is typically characterized by AM-AM (amplitude to amplitude) modulation curves which reflect the amplifier's gain progression as a function of the input power. At low input power levels, the output power is a linearly scaled version of the input power level. At higher input power levels, the scaling of output to input power becomes non-linear and the results become similar to the results derived from the two-tone excitation test. The non-linear behavior produces fundamental, third harmonic, and fifth harmonic responses along with inter-modulation terms which are a function of the input power level. The output waveform for the amplifier can be written as a sinusoid with an envelope constructed from the fundamental, third, and fifth harmonics and a phase component which is a function of the modulation signal.

$$v_s = \{cos\omega_m t + \mu_3 cos3\omega_m t + \mu_5 cos5\omega_m t\} * \cos\{\omega t + \frac{\emptyset}{2}(1 + cos2\omega_m t)\} \quad (2.5)$$

$\omega_m = frequency\ of\ the\ modulating\ signal$
$\omega = frequency\ fo\ the\ carrier\ signal$
$\mu_3, \mu_5 = amplitude\ fo\ the\ 3^{rd} and\ 5^{th}\ harmonics$
$\emptyset = peak\ magnitude\ of\ the\ AM - PM\ shift$

The output signal can be simplified and expressed as:

$$v_s = \frac{1}{2}\cos\left\{(\omega \pm \omega_m)t - \frac{\emptyset}{2}\right\} + \frac{\emptyset}{8}\{\sin(\omega \pm \omega_m)\, t + \sin(\omega \pm 3\omega_m)\, t\} + \frac{\mu_3}{2}\cos\left\{(\omega \pm 3\omega_m)t - \frac{\emptyset}{2}\right\} \quad (2.6)$$

$$+\frac{\emptyset\mu_3}{8}\{\sin(\omega \pm 3\omega_m)t + \sin(\omega \pm 5\omega_m)\,t\}$$

The terms that produce the third order inter-modulation response consist of a phase distortion component and an amplitude distortion component. The AM-AM and AM-PM components will always combine to produce IM_3 sidebands which have greater amplitude than either of the individual components. The coefficient "μ_3" denotes the AM-AM component of the IM_3 response and the coefficient "$\frac{\emptyset}{8}$" denotes the AM-PM component. The cross product terms "$\frac{\emptyset\mu_3}{8}$" presented in the previous equations are assumed to be negligible and that portion of the equation can be ignored.

$$v_{m3} = \frac{\mu_3}{2}\cos\left\{(\omega \pm 3\omega_m)t - \frac{\emptyset}{2}\right\} + \frac{\emptyset}{8}\sin(\omega \pm 3\omega_m)\,t \qquad (2.7)$$

2.2.2 AM-PM Effects

AM-PM effects can be defined as a change in the phase response of an amplifier due to the increase in amplitude of the input signal. AM-PM effects can be traced to the signal level dependency of several key transistor elements. For Field Effect Transistors, the input capacitance and the resistance associated with

the parasitic gate to source transistor are those elements. All of these effects are detailed, interactive, and highly complex and are hard to model. AM-PM effects can be modeled concisely by making some key assumptions based on physical observations [9]. Assuming that the transistor is excited by a sinusoid with a variable amplitude envelope, the phase response exhibits a fundamental frequency which is twice that of the double side-band modulation waveform.

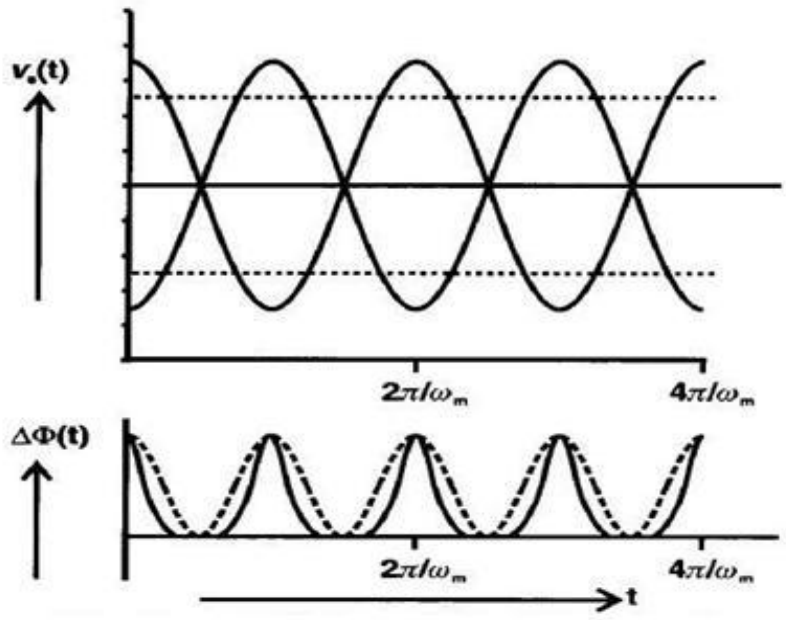

Figure 2.3- Envelope and AM-PM phase variation [11]

From the graph presented above, it is assumed that the output of the amplifier can be expressed as:

$$v_s = \cos(\omega_m t)\cos\left\{\omega t + \frac{\emptyset}{2}(1 + cos2\omega_m t)\right\} \quad (2.8)$$

$\omega_m = frequency\ of\ the\ modulation\ signal$
$\omega = carrier\ frequency$
$\emptyset = peak\ magnitude\ of\ AM - PM\ shift$

making the substitution:

$$\Psi = \frac{\emptyset}{2}(1 + \cos2\omega_m t) \quad (2.9)$$

$$cos\Psi = 1 \quad (2.10)$$

$$sin\Psi = \Psi \quad (2.11)$$

$$\emptyset \ll 1$$

The amplifier output voltage can be expressed as:

$$v_s = \cos(\omega_m t)\{\cos(\omega t)\, cos\Psi - \sin(\omega t)\, sin\Psi\} \quad (2.12)$$
$$= \cos(\omega_m t)\{\cos(\omega t) - \sin(\omega t)\,\Psi\}$$

which simplifies to:

$$v_s = \frac{1}{2}\cos\left\{(\omega \pm \omega_m)t - \frac{\emptyset}{2}\right\}$$
$$+\frac{\emptyset}{8}\{\sin(\omega \pm \omega_m)\, t + \sin(\omega \pm 3\omega_m)\, t\} \quad (2.13)$$

The AM-PM distortion produces additional terms at the same frequency as the third order inter-modulation products, $\omega \pm 3\omega_m$. These additional terms will have an amplitude of "$\frac{\emptyset}{8}$" and will add vectorially to the third order inter modulation terms produced by the amplitude distortion. The key point is that AM-AM and AM-PM effects contribute to the IM_3 response to the two tone test. It is important to note this when evaluating the effectiveness of the Doherty configuration

2.3 Efficiency and Linearity Enhancement for Power Amplifiers

The amplification of AM RF signals has two inherent problems. First, the modulated signal will be distorted if the amplifier is operated at its full rated RF power level. Second, power amplifiers only give maximum efficiency at a single power level which is usually near the maximum rated power level of the device. As the input power level is backed off, the amplifier gain behaves linearly but the efficiency decreases significantly.

The solution to the linearity problem requires that the transfer characteristics of the amplifier be made more linear over a given power range. Higher linearity usually comes at the cost of lower efficiency and baseband frequency limitations. Several efficiency techniques were developed in the early era of radio broadcasting. These techniques fall into one of three categories; the Doherty Amplifier, the Outphasing Amplifier, and the Envelope Elimination and Restoration technique [11]. The discussion will start with examining the relationship between the load impedance values and peak efficiency. The output -load of an ideal power amplifier consist of a load resistance at the fundamental frequency and a shunt resonator which provides a short circuit at all harmonics. The load resistor is chosen based on the family of curves for a given device. The

following discussion assumes a class A configuration. The optimum load impedance is given by:

$$R_{opt} = 2\frac{V_{supply}}{I_{max}} \qquad (2.14)$$

The device is biased such that the quiescent current is half of the maximum current. These conditions are chosen such that the output voltage has maximum swing when driven at the edge of saturation.

$$P_{OUT} = \frac{V_{supply} I_{max}}{4} \qquad (2.15)$$

$$P_{DC} = \frac{V_{supply} I_{max}}{2} \qquad (2.16)$$

$$\eta_{efficiency} = \frac{P_{out}}{P_{DC}} \cong 50\% \text{ (Class A)} \qquad (2.17)$$

As the input power to the amplifier is reduced, the output swing and the current delivered to the load impedance drops. The DC bias point remains constant hence the overall efficiency of the amplifier decreases as the output power is no longer operated at its maximum rated power. If the load resistance could be made to dynamically change with the input power, the maximum efficiency could be maintained. If the load impedance is changed, extra precautions have to be taken in order to maintain a constant gain. The drive dependent resistor and the linearity issue can be solved simultaneously using a configuration of two separate amplifiers. Doherty's invention only changes the

load resistor value optimally for a few dB of back off from the maximum power level, but it solves the linearity issue elegantly at the same time.

Chapter 3: Methods

3.1 Doherty Purpose and Concept

The Doherty amplifier was developed in 1936 as an efficiency enhancement technique. This technique addressed the key problem of maintaining high efficiency at output power levels slightly lower than the maximum rated level.

The Doherty amplifier uses what is commonly known as active load pulling.

The load resistance or reactance of the RF load can be altered by applying current from a second source [12].

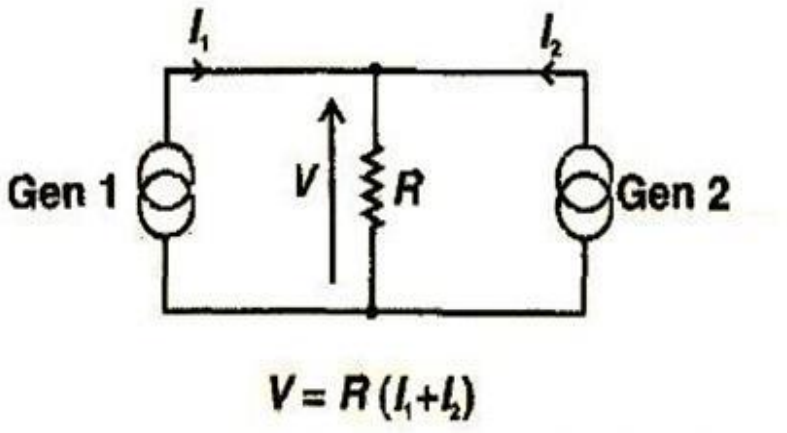

Figure 3.1-Active loadpull simplified schematic [16]

The basic model in Fig. 3.1 illustrates the idea of active load pulling. The equivalent impedance seen by each current generator in the above model is influenced by the magnitude of the other generator. The voltage on the load resister "R" is:

$$V_L = R(I_1 + I_2) \qquad (3.1)$$

The equivalent impedance seen by the first current generator is:

$$R_1 = \frac{V_L}{I_1} = R\left(1 + \frac{I_2}{I_1}\right) \qquad (3.2)$$

Likewise, the equivalent impedance seen by the second current generator is given by:

$$R_2 = \frac{V_L}{I_2} = \left(1 + \frac{I_1}{I_2}\right) \qquad (3.3)$$

The equations above show the various impedances can be pulled by varying magnitude of the opposite current generator. The two current generators can be replaced by transistors with co-phased input driving signals. The output characteristics of the transistors used in this type of configuration can be tailored based on the variation of size and bias level of the devices used.

The basic concept of the Doherty amplifier is illustrated in the Fig.3.2. The two devices will be called "main" and "auxiliary". The maximum rated output power for this configuration is a combination of the power of both devices. At

maximum output power, both devices are operating. As the output power is backed off from its maximum rating, both devices will operate until an Output Back Off power point is reached (OPBO). At this point, the auxiliary amplifier shuts off and the main amplifier operates alone. The OPBO point is chosen at the point where the main amplifier has its maximum gain. This point also coincides with point where the main amplifier starts to compress as seen in Fig.3.3. As the main amplifier starts to go into compression, the auxiliary amplifier begins to actively pull the load impedance. The net result of the active load pulling is the main amplifier operates at maximum efficiency and the output power of the auxiliary amplifier increases proportional to the cube of the input power. The combination of the main and auxiliary amplifiers produces a power gain that is linear over a large input power range and gives maximum efficiency at Output Back Off Power points which are several dB lower than the maximum rated output power.

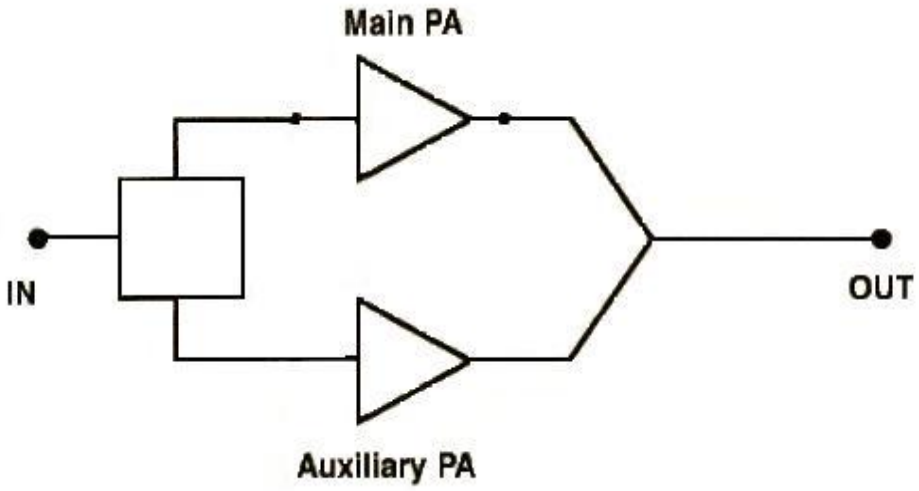

Figure 3.2-Doherty Simplified schematic

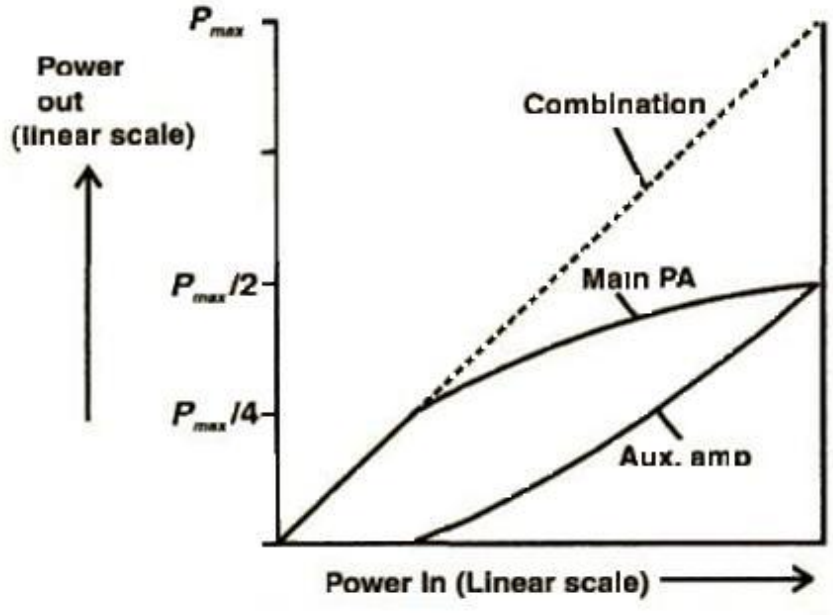

Figure 3.3-Doherty Basic Operation [11]

A simplified schematic of the Doherty amplifier is presented in figure 3.4 [13]. The current generators have been replaced by devices and a quarter wave transmission line is inserted between the load impedance and the main current generator. The quarter wave transmission line functions as a impedance inverter for the actively pulled load impedance.

In the output power region, 6 dB OPBO to maximum output power, the device currents can be represented as:

$$I_1 = \frac{I_{max}}{4}(1 + \xi) \qquad (3.4)$$

$$I_2 = \frac{I_{max}}{2}\xi \qquad (3.5)$$

$\xi = arbitrary\ symbol\ with\ a\ value\ between\ 0\ and\ 1$
$I_{max} = maximum\ linear\ current\ swing$

It is assumed that both devices have the same maximum linear current swing I_{max}. Based on the previous argument, the equivalent impedance seen by device number two and the impedance at one end of the quarter wave transmission line is:

$$Z_{1T} = \frac{R_{opt}}{2}\left(1 + \frac{I_2}{I_{1T}}\right) \qquad (3.6)$$

$$Z_2 = \frac{R_{opt}}{2}\left(1 + \frac{I_{1T}}{I_2}\right) \qquad (3.7)$$

The maximum output power condition will be defined as the point at which $I_{1T} = I_2$. At this point, the impedance seen by device number two and the impedance at one end of the quarter wave impedance transformer is $\frac{R_{opt}}{2}$.

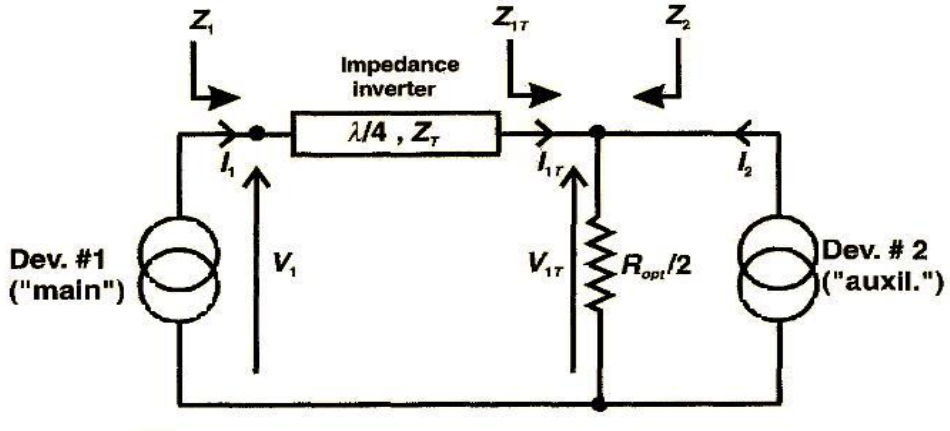

Figure 3.4-Active loadpull and Doherty simplified schematic combined [11]

The impedance seen looking into a transmission line terminated by a load impedance Z_L is:

$$Z_{IN}(d) = Z_0 \frac{Z_L \cos(\beta d) + jZ_0 \sin(\beta d)}{Z_0 \cos(\beta d) + jZ_L \sin(\beta d)} \qquad (3.8)$$

For a quarter wave transmission line, the quantity "βd" reduces to "$\frac{\pi}{2}$". The input impedance for the quarter wave transmission line becomes:

$$Z_{IN}\left(\frac{\lambda}{4}\right) = {Z_0^2}/{Z_L} \qquad (3.9)$$

For the structure in figure four, the characteristic impedance "Z_0" becomes "Z_T" and load impedance becomes "Z_{1T}". The equivalent impedance at the output of device one is given by:

$$Z_1 = {2Z_T^2}\Big/{R_{opt}(1+\frac{I_2}{I_{1T}})} \qquad (3.10)$$

$$= {2Z_T^2}\Big/{R_{opt}(1+\frac{I_2 Z_T}{V_1})}$$

The voltage at the output of the main device can now be expressed as:

$$V_1 = I_1 Z_1 \qquad (3.11)$$

$$= {2I_1 Z_T^2}\Big/{R_{opt}(1+\frac{I_2 Z_T}{V_1})}$$

If the equations for I_1 and I_2 are used, V_1 reduces to:

$$V_1 = \left(\frac{Z_1}{R_{OPT}}\right)\left(\frac{I_{max}}{2}\right)[Z_T + \xi(Z_T - R_{OPT})] \qquad (3.12)$$

If the characteristic impedance of the quarter wave transmission line is set equal to the optimum load impedance, R_{OPT}, then the output voltage of the main device becomes independent of "ξ" and remains constant from 6dB OPBO up to the maximum rated output power point.

$$V_1 = R_{OPT}\left(\frac{I_{max}}{2}\right) \qquad (3.13)$$

As mentioned previously, the combined output power continues to increase because of the contribution of the auxiliary amplifier in this region. The output power will increase linearly until the auxiliary amplifier starts to compress.

3.2 Doherty Implementation

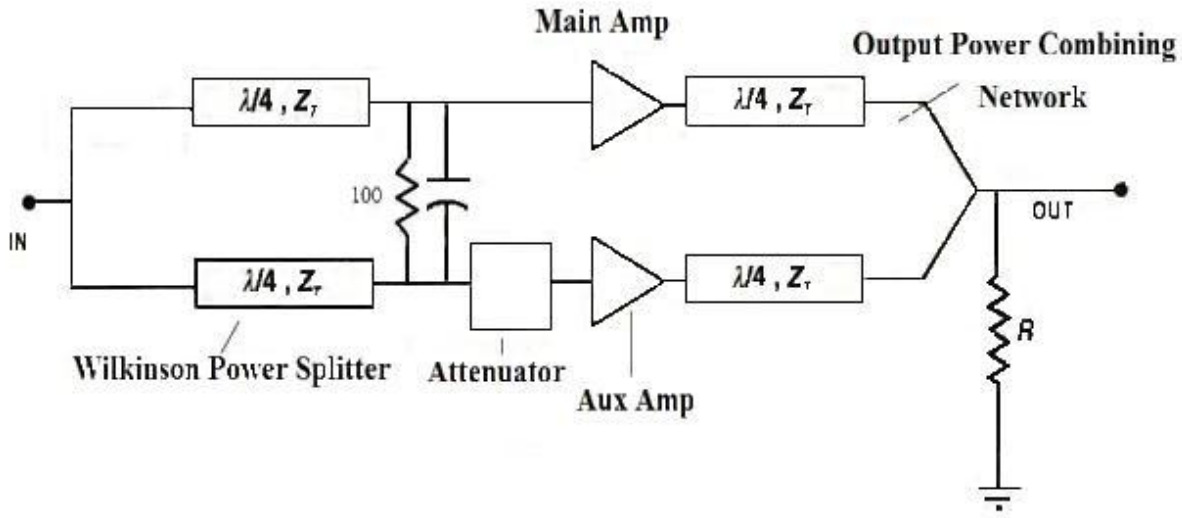

Figure 3.5-Doherty Block level schematic

The final Doherty configuration consists of a Wilkinson power splitter, an attenuator, the main and auxiliary amplifiers, and the power combining networks. The Wilkinson power splitter used in this implementation is a quarter wave lumped element realization. The power splitter produces co-phase signals

with equal amplitude and provides good isolation between the output ports. The low pass π network was used since it consumes less space and filters the higher order harmonics of the input signal. The characteristic impedance for each port was designed for 50Ω.

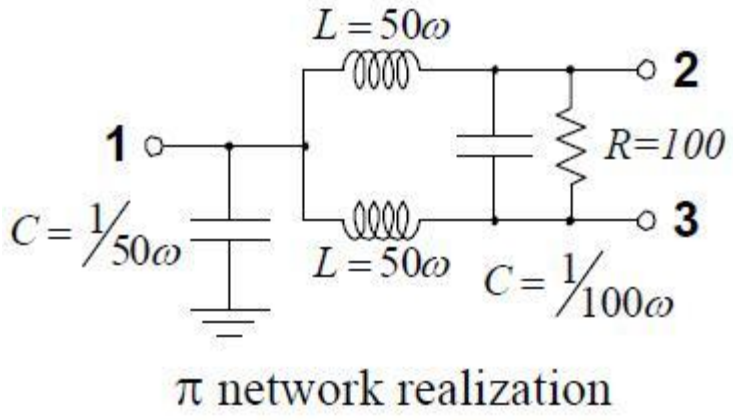

Figure 3.6 Wilkinson Power Splitter Schematic

The attenuator portion of the circuit is connected between the power splitter and the auxiliary amplifier. This block shifts the turn on point for the auxiliary amplifier. The auxiliary amplifier is a class "C" amplifier and its "DC" operating point is the cutoff region of the transistor. The turn on point for the auxiliary amplifier tailored to give the best gain linearity for the composite Doherty structure.

$$R_3 = \left. 2\sqrt{Z_{IN} Z_{OUT} 10^{\frac{L}{10}}} \right/ (10^{\frac{L}{10}} - 1) \quad (3.13)$$

$$R_1 = \left(\frac{10^{\frac{L}{10}} + 1}{10^{\frac{L}{10}} - 1} \right) Z_{OUT} - R_3 \quad (3.14)$$

$$R_2 = \left(\frac{10^{\frac{L}{10}} + 1}{10^{\frac{L}{10}} - 1} \right) Z_{OUT} - R_3 \quad (3.15)$$

L=desired loss in dB
Z_{IN}=desired input impedance (ohms)
Z_{OUT}=desired output impedance (ohms)

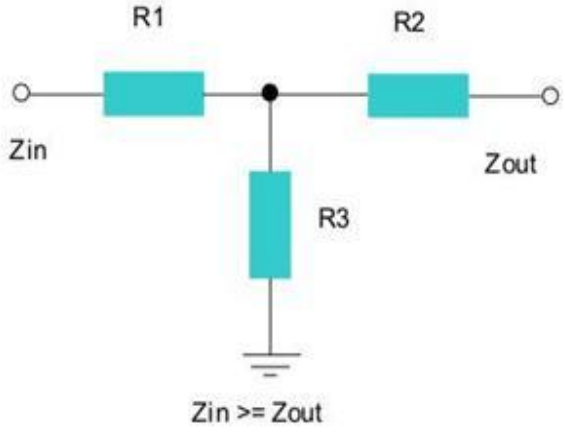

Figure 3.7-3dB Attenuator Schematic

The main amplifier is a class A structure. This type of amplifier is very linear over a large output power range and has reasonable power efficiency at the maximum rated output power. The output matching network consists of a pull up inductor, a DC block cap, and the π network equivalent of a quarter wave

transmission line. The pull up inductor is used to resonate out the drain to source capacitance C_{DS} at operating frequency. The output impedance is completely real at the operating frequency as a result of the pull up inductor [15].

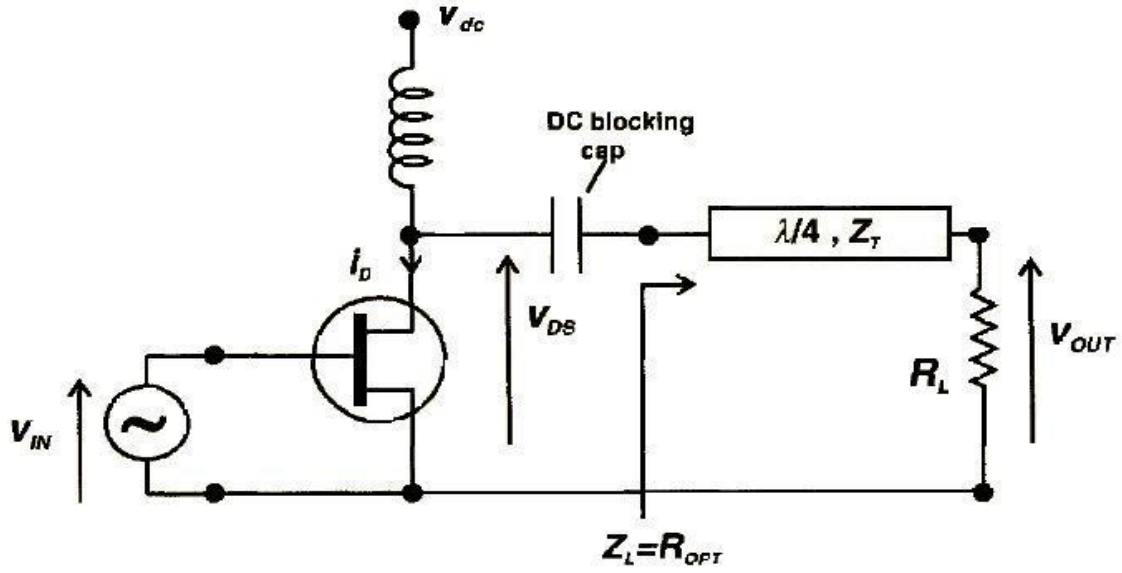

Figure 3.8-Class A Amplifier Simplified Schematic [11]

The figure above illustrates the basic configuration of the class A amplifier. The dc blocking cap is used to provide charge to the equivalent optimum load impedance. This load impedance is determined from the family of curves for the device. The parallel combination of the output impedance of the device and the impedance presented at the other end of the dc blocking cap will form the optimum load impedance. The actual load impedance for the Doherty amplifier is 50Ω's since the device has to drive a network analyzer. The 50Ω load is

transformed into a optimum load impedance via the π network equivalent of the quarter wave transmission line [14].

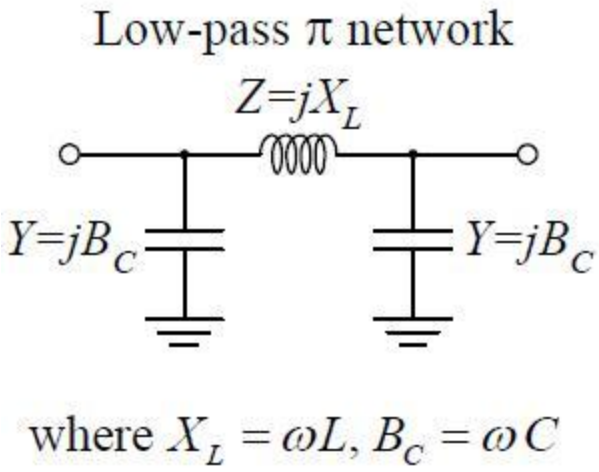

Figure 3.9-Transmission Line Quarter wave Low Pass equivalent

The input match for the class A amplifier is a simple high pass "L" network. The dc gait bias ,"V_G ", is connected to the inductor and the input signal is applied directly to the cap.

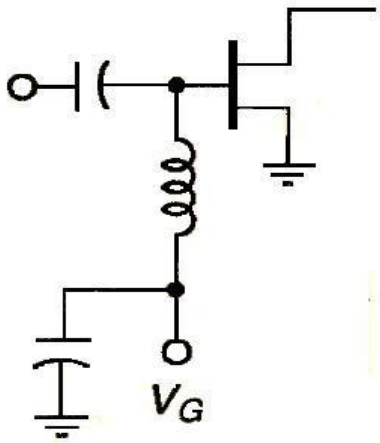

Figure 3.10-Input Matching Network [3]

The class "C" amplifier has an identical structure to the class A amplifier. The main difference is that the dc operating point for the transistor is in the cutoff region and the optimum load impedance for the class "C" amplifier is different.

Chapter 4: Implementation

4.1 Introduction

The final design was implemented in Triquent's .5um GaAs TQPED process. The TQPED process provides both E-Mode pHEMT devices and D-Mode transistors on the same wafer. The process is targeted for linear power amplifiers, low noise amplifiers, and RF switches. This process offers a D-Mode pHEMT with a -.8V pinch off voltage and an E-Mode pHEMT with a .35V threshold voltage. The process also offers three metal interconnecting layers, precision NiCr resistors, high value MIM capacitors and high Q inductors.

The design implementation consist of Class A amplifier, a Class C amplifier,
A Wilkinson power splitter, a 3 dB attenuator and a Class A driver amplifier.
The Class A and C amplifiers make up the Doherty structure and are connected at the input via the power splitter and the 3 dB attenuator. These amplifiers are connected at the output via quarter wave transmission line equivalent circuits and a 50 Ohm load. D-Mode pHEMT devices were used to design the amplifiers that make up the Doherty structure. A driver amplifier was added to the design for testing purposes. This amplifier is a Class A structures designed with an E-Mode pHEMT device.

4.2 Components

4.2.1 Class A Amplifier

The schematic for the class A amplifier is presented in figure 2. The D-Mode pHEMT device is biased at Vgate=-0.1V and Vdrain=8V.

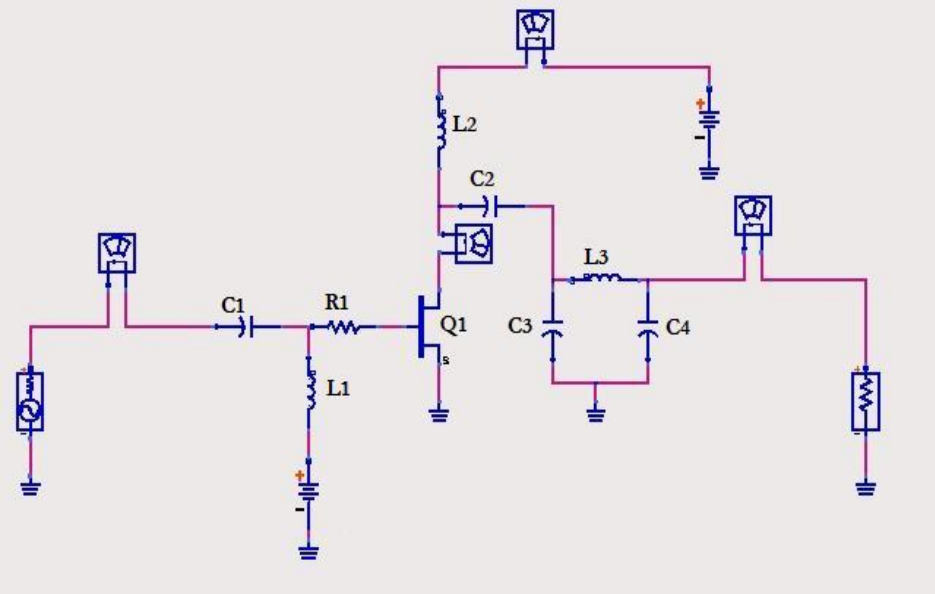

Figure 4.1-Class A Amplifier Schematic

The general procedure for designing the output network consist of resonating out the drain to source capacitance to produce a real impedance at the drain of the device. Next, a DC blocking capacitor is connected between the drain of the transistor and the impedance transformer for the device. The impedance transformer is a low pass quarter wave equivalent circuit used to shift the

50Ohm load to the Cripps load value. The resulting output network consist of a pull up inductor which is used to resonate out the drain capacitance, a 20pF dc blocking cap, and the low pass quarter wave equivalent network.

The input matching network for the Class A amplifier consist of a series stabilizing resister, and an L-network which functions as a matching network and a dc feed for the gate bias.

4.2.2 Class C Amplifier

The implementation of the class C amplifier is very similar to that of the class A structure. An inductor is used to resonate out the drain to source capacitance and the quarter-wave transmission line equivalent is used to transform the load impedance into a value that yields maximum output power. Since the primary purpose of the auxiliary amplifier is to actively pull the load impedance for the main amplifier, efficiency and gain are not as important as the maximum rated output power and the output power saturation point. The quarter-wave impedance transformer values are essentially the same as those for the class A amplifier but the gain of the amplifier is significantly lower because the device is biased near the cut-off region.

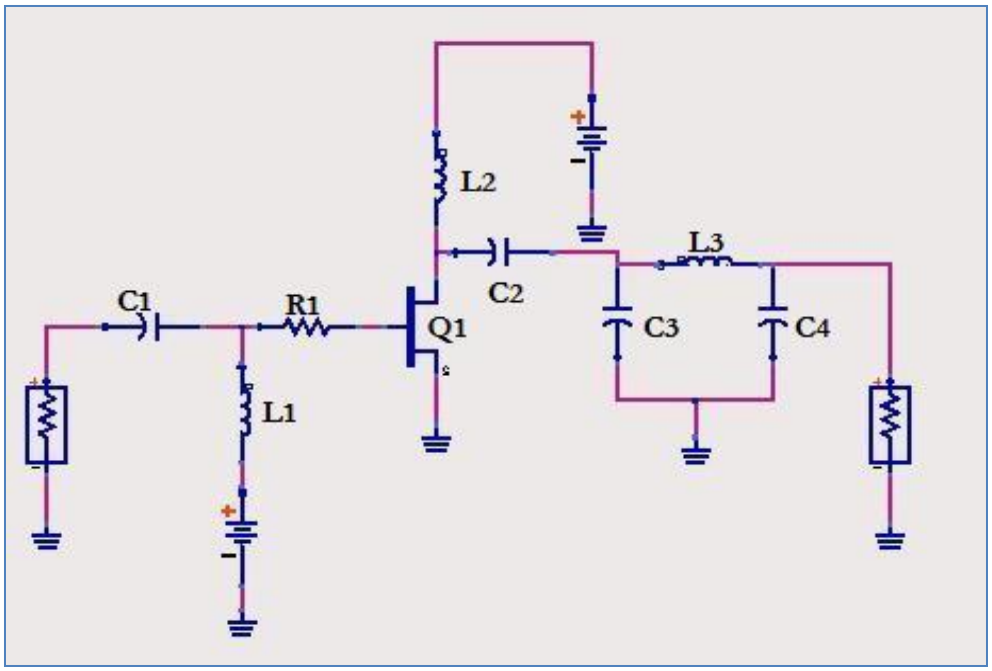

Figure 4.2-Class C Amplifier Schematic

4.2.3 Driver Amplifier

The driver amplifier is included in the design purely for testing purposes. A high frequency source with a 25dB to 30dB output was needed to push the Doherty configuration into saturation. Unfortunately that source was not available hence another gain stage was added in order to compress the structure before the 20dB limit of my source was reached. A schematic of the driver amplifier is presented below.

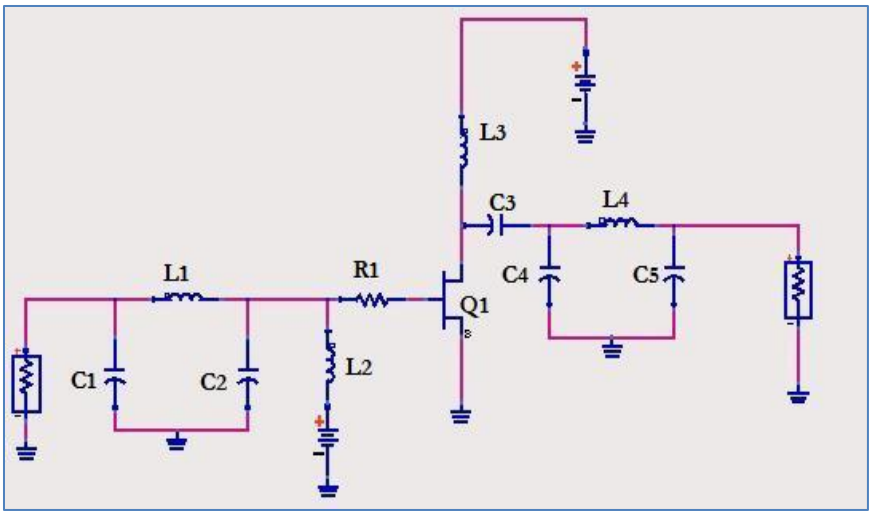

Figure 4.3-Driver Amplifier Schematic

The construction of the output network is generally the same as the other amplifiers. First, the optimum load impedance is calculated from the dynamic load line simulation. The next step in constructing the output network is to resonate out the drain to source capacitance and provide an impedance transforming network for optimum load conditions. Next, a series stabilizing resistor and a shunt inductor are placed at the input of the device along with an impedance transforming network to match to a 50 Ohm input load.

4.2.4 Wilkinson Power Splitter

The schematic for the Wilkinson Power splitter is given in the figure below. The circuit was designed for an equal power split at 5GHz and 50 Ohm terminations at each port.

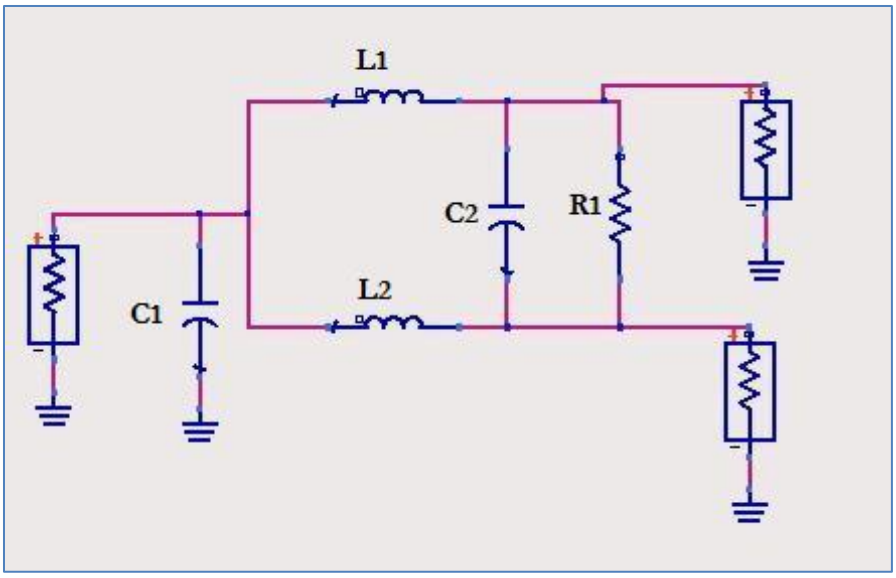

Figure 4.4-Wilkinson Power Splitter Schematic

4.2.5 3dB Attenuator

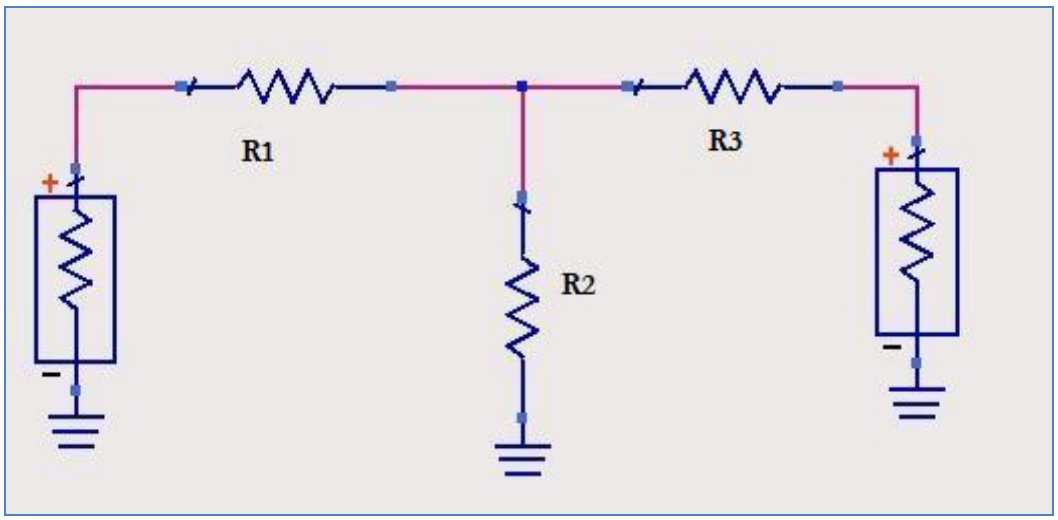

Figure 4.5-Attenuator Schematic

The schematic for the 3dB attenuator is shown above. The design equations for the circuit were presented in the previous chapter.

4.3 Component Simulation Results

4.3.1 Class A Amp Simulation Results

The optimum load is determined from the dynamic load line simulation.

In this case figure 4.6 shows that the optimum load impedance is approximately 66 Ohms. Figure 4.7 shows S_{22} after the drain capacitance has been resonated out.

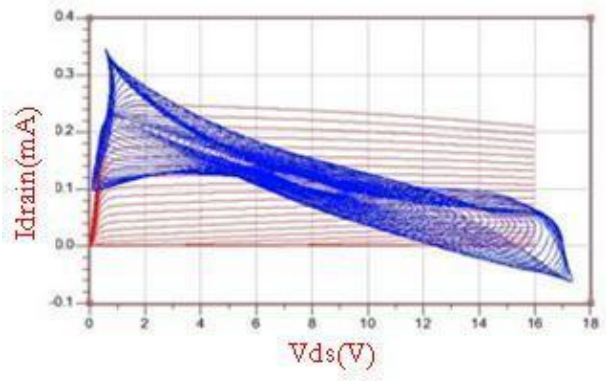

Figure 4.6-Dynamic Load Line for Class A Amplifier

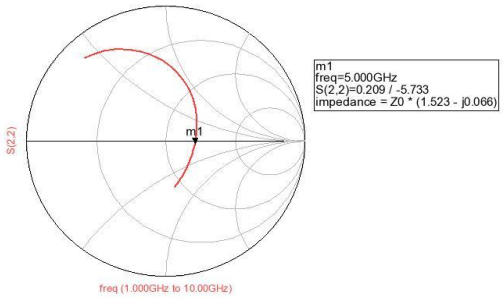

Figure 4.7-S_{22} for Class A

The input and output stability curves and S_{11} curve post output match are presented in figures 4.8 and 4.9.

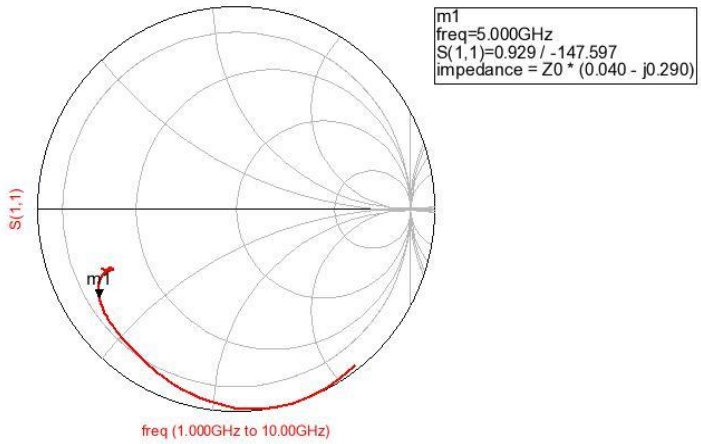

Figure 4.8-Pre-Matched S_{11} for Class A Amplifier

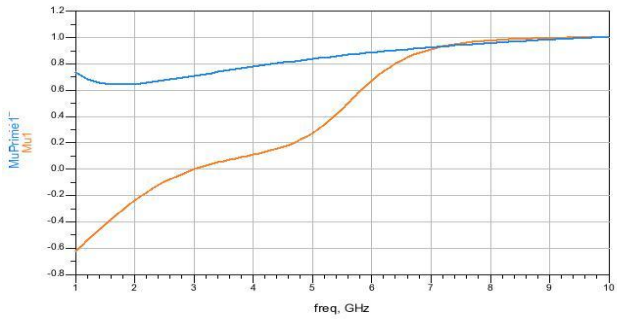

Figure 4.9-Stability Curves without Stabilizing Resister for Class A

A Mu1 value which is less than "1" indicates that the amplifier is unstable and will oscillate as mentioned by Edwards et al [16] [17]. A series or shunt resister placed at the input or output of the device will stabilize the circuit and push both "Mu" and "Mu1" values above unity. A resistor placed at the output of the device will limit the voltage delivered to the load and lower the Power Added

Efficiency. Therefore, the stabilization resistor is placed at the input of the device and the resulting response is presented below. The input and output stability parameters are both above unity and input impedance of amplifier is inside the Smith Chart for the frequencies of interest.

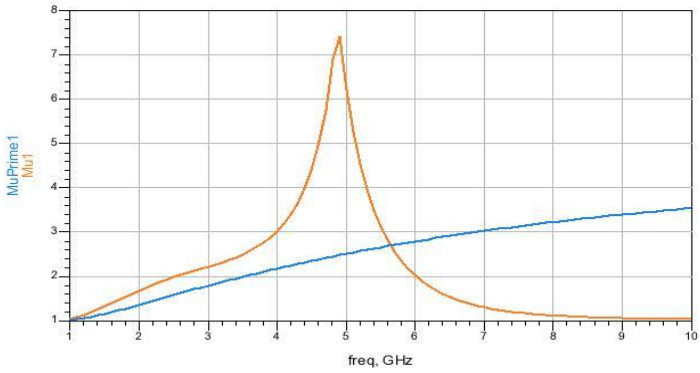

Figure 4.10-Stability Curves with Series Stabilizing Resistor

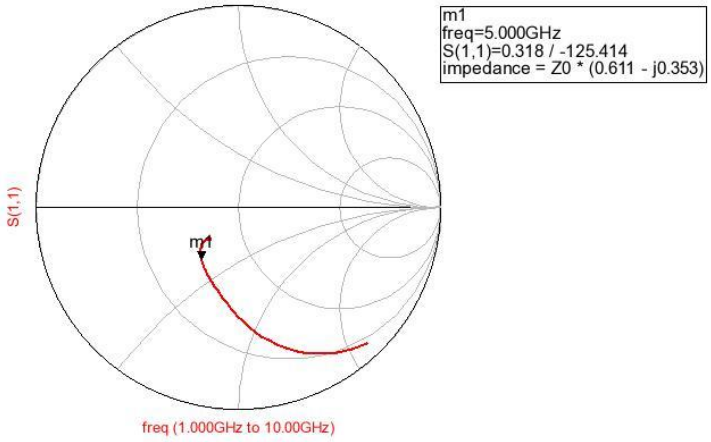

Figure 4.11- S_{11} with Series Stabilizing Resister Added

The input matching circuit is a high-pass "L" shaped network consisting of a series capacitor and shunt inductor. The "L" shaped network is connected to the stabilizing resistor and the resulting S-parameter are:

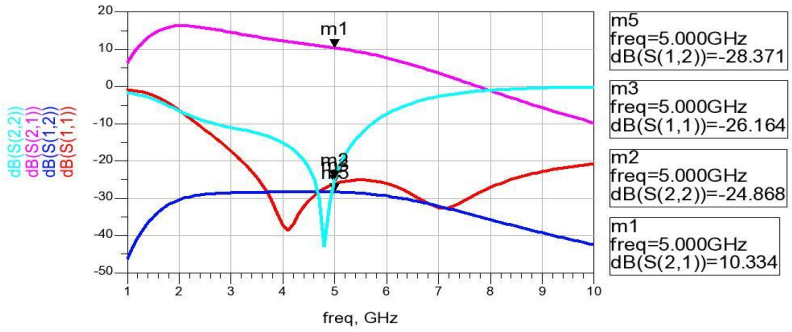

Figure 4.12- Final S-Parameters with Output Network and Input Match

The harmonic balance simulation results for the Class A Amp are presented below. Figure 4.13 shows output power versus input power with the compression points labeled on the graph. Figure 4.14 shows the Power Added Efficiency versus input power.

Figure 4.13-P_{out} versus P_{in} for Class A Amplifier

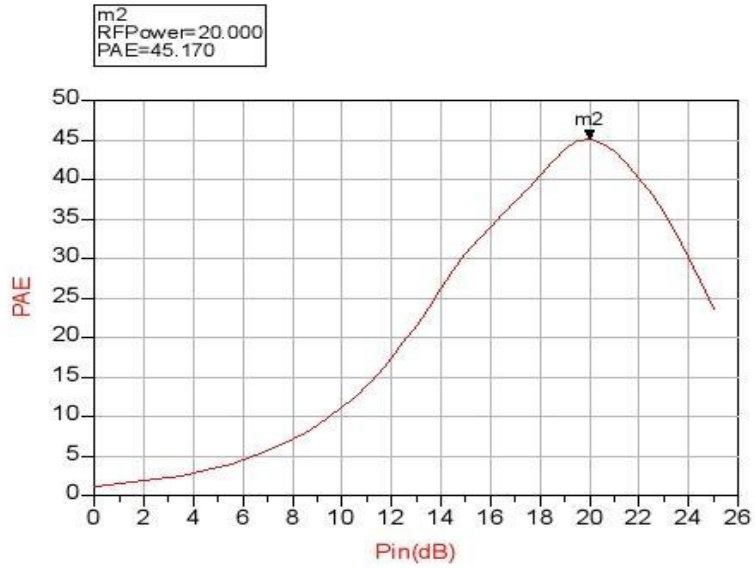

Figure 4.14-PAE for Class A Amplifier

4.3.2 Class C Amp Simulation Results

The input power versus output power curve is shown below. The amplifier saturates at an output power of 27dB and exhibits a power gain which is dependent on the input power level.

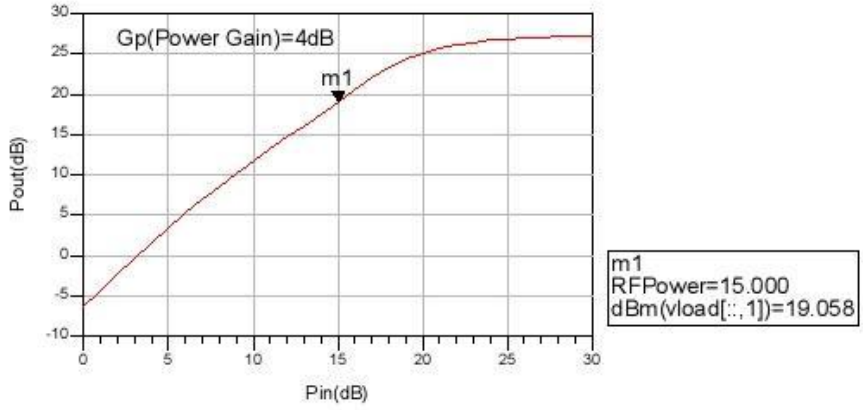

Figure 4.15-Pout versus Pin for Class C Amplifier

The figure below shows the drain voltage and current for the class C amplifier. At lower input power levels, the drain current is on for more than half of the output voltage cycle. As the input power level increases, the drain current is on for about half of the output voltage cycle. At these high input drive levels, the amplifier approaches true class C operation.

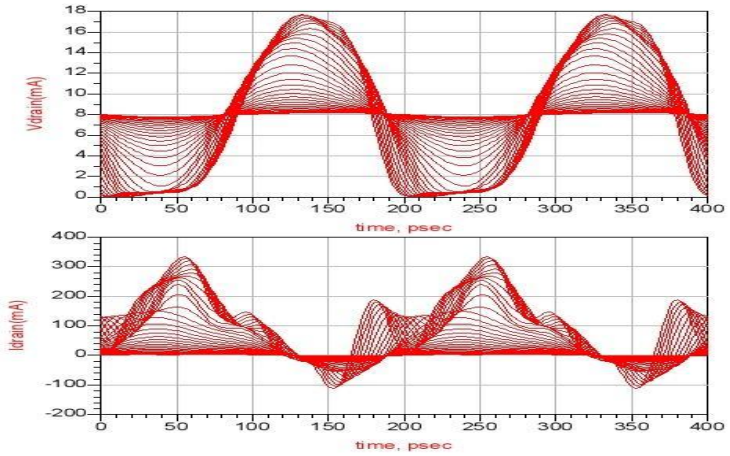

Figure 4.16-Drain Voltage and Current for Class C Amplifier

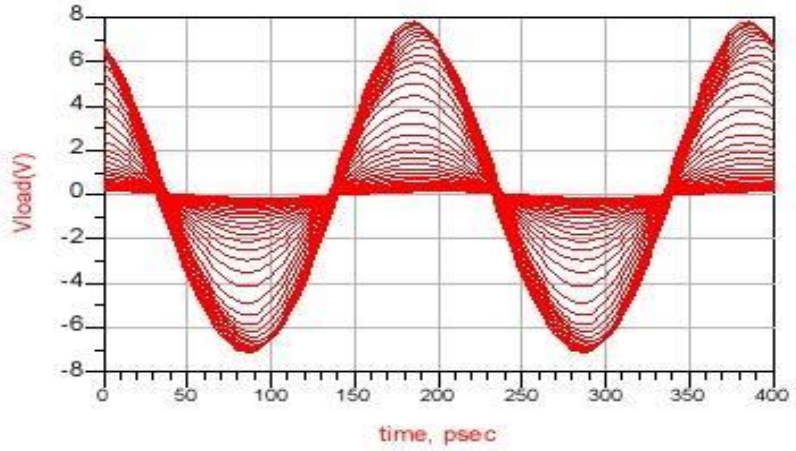

Figure 4.17-Load Voltage for Class C Amplifier

The final S-parameter curves for the class C amplifier and the input and output stability curves are presented in figures 4.18 and 4.19. The S-parameter data shows a good input match at 5GHz. The output match is poor as expected since the design goal is for maximum power. The power gain numbers are reasonable at 5GHz. The optimal frequency for this process is around 2GHz and S_{21} starts to roll of after this frequency.

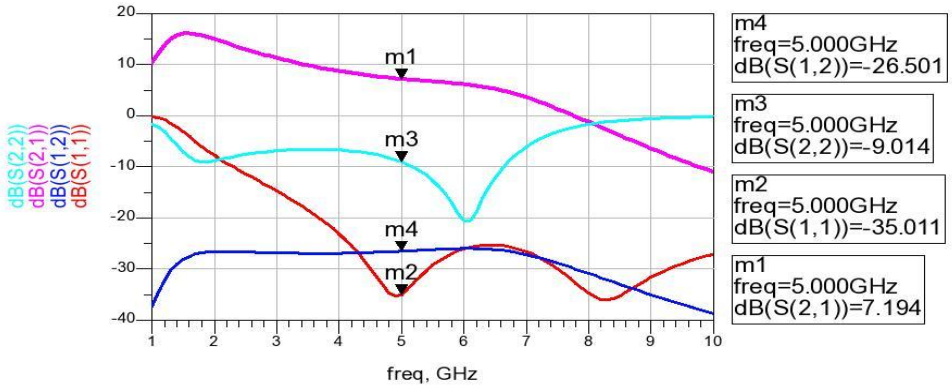

Figure 4.18-Class C S-Parameters

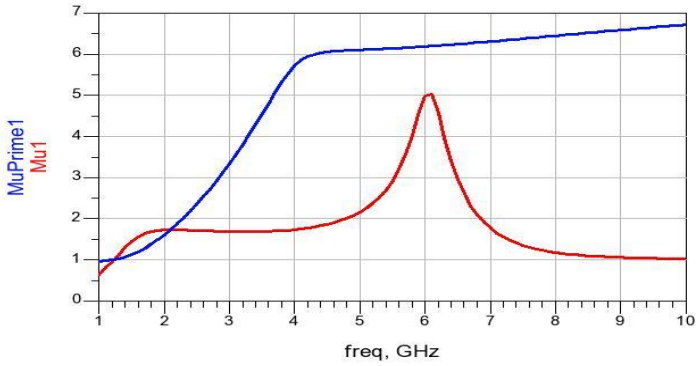

Figure 4.19-Class C Stability Curves

4.3.3 Driver Amplifier Simulation Results

First, the optimum load impedance is calculated from the dynamic load line simulation. The value for the optimum load is approximately 60 Ohms.

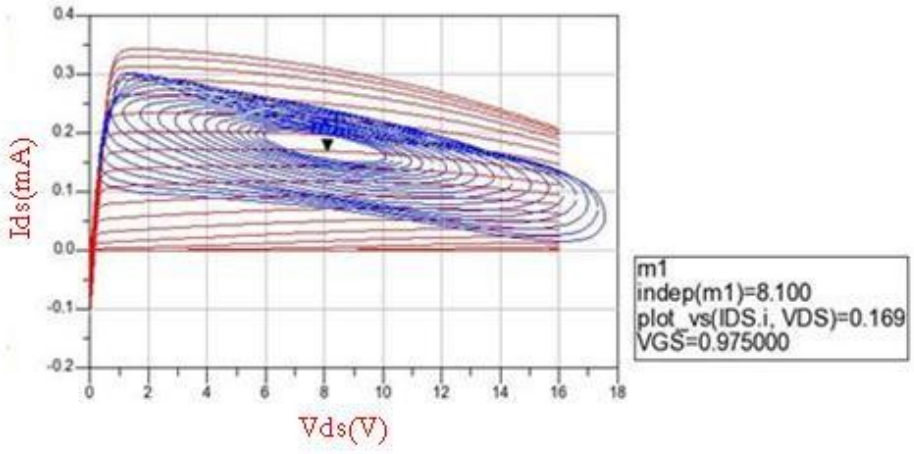

Figure 4.20-Dynamic Load Line for Driver Amplifier

Figure 22 shows the S_{22} for the amplifier after the pull up inductor is placed in the circuit. The stability curves for the amplifier show that it is unstable over a large frequency. A series stabilizing resistor and a shunt inductor are placed at the input of the device along with impedance transforming network at the output. The resulting S_{11}, S_{22}, and stability curves are presented in figures 4.21 and 4.22.

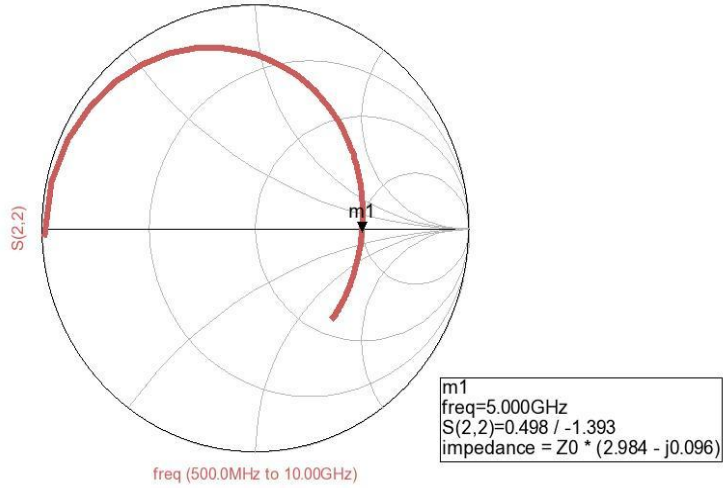

Figure 4.21-S_{22} for Driver Amplifier

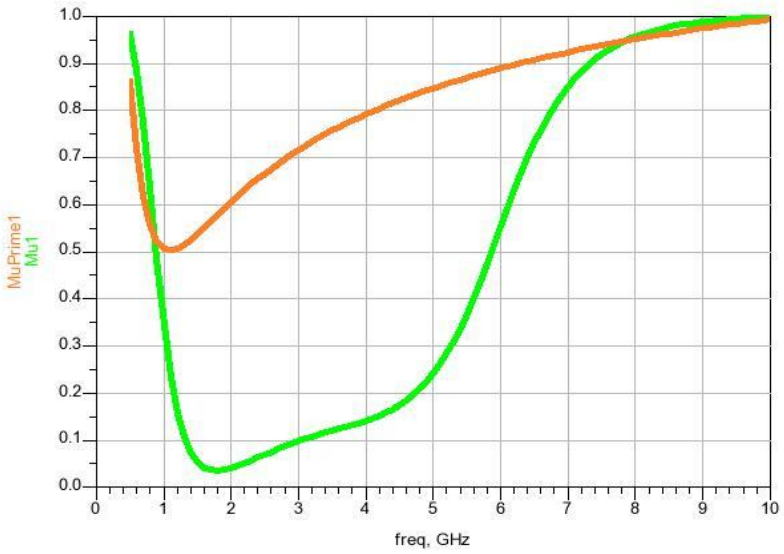

Figure 4.22-Stability Curves before Series Resistor Addition

Since the resulting S_{11} parameter represents a input impedance which is purely real, an impedance transforming network is used to match to a 50 Ohm input.

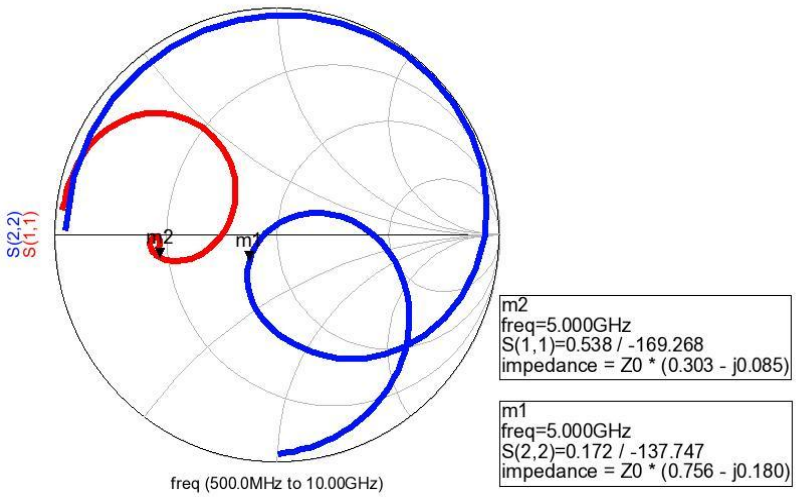

Figure 4.23-S_{11} and S_{22} after Stabilization

The final S-parameters and stability response are presented in the following figures. The S-parameters show a reasonable input and output match at 5 GHz and a power gain close to 18dB at the operating frequency. The amplifier is unconditionally stable from 2.5GHz to 5GHz and conditionally stable in the 1GHz to 2.5GHz range. The output power versus input power curve also shows a power gain close to 18dB and a 1dB compression point at an output power of 24.5dB.

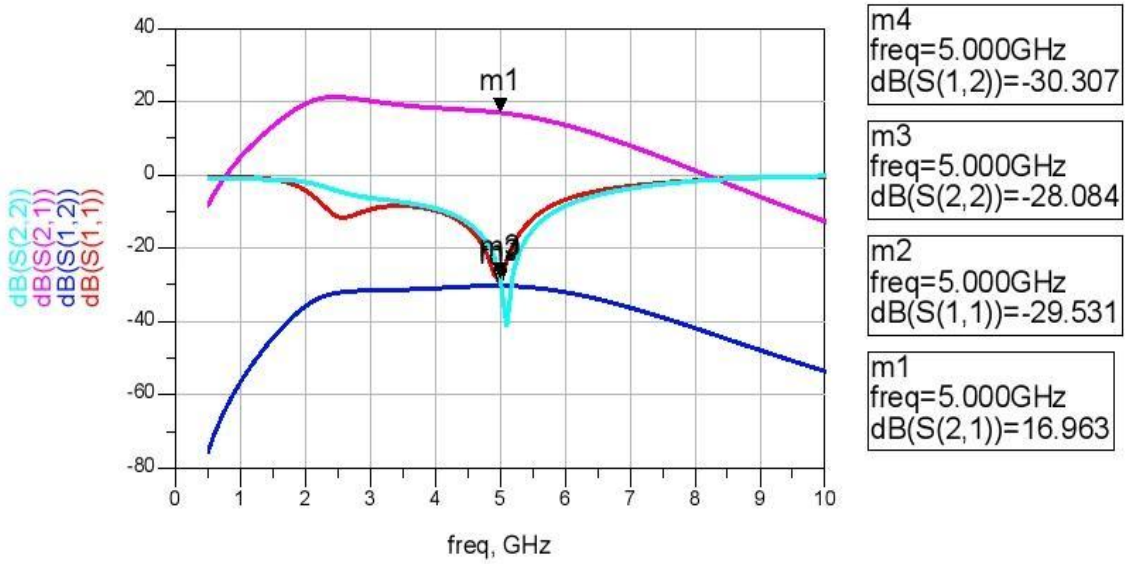

Figure 4.24-Final S-Parameters for Driver Amplifier

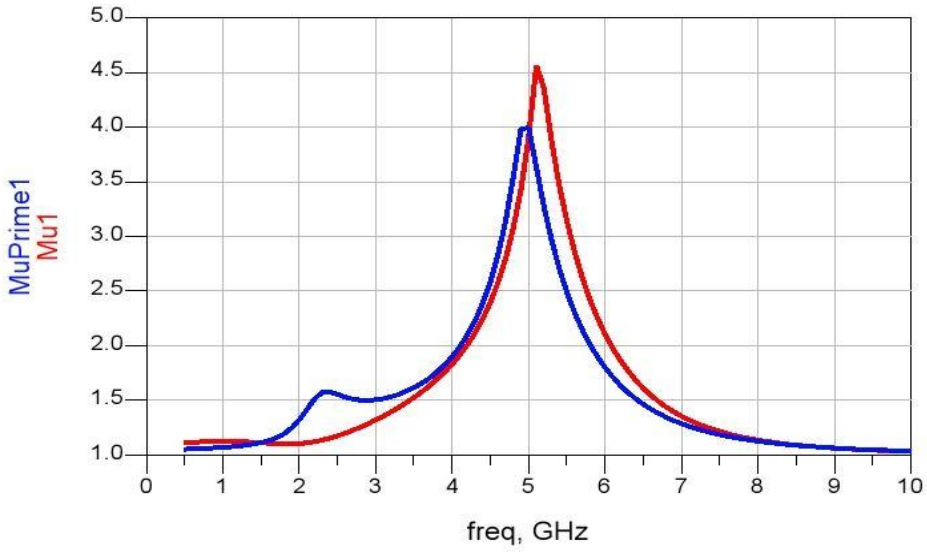

Figure 4.25-Final Stability Curves for Driver Amplifier

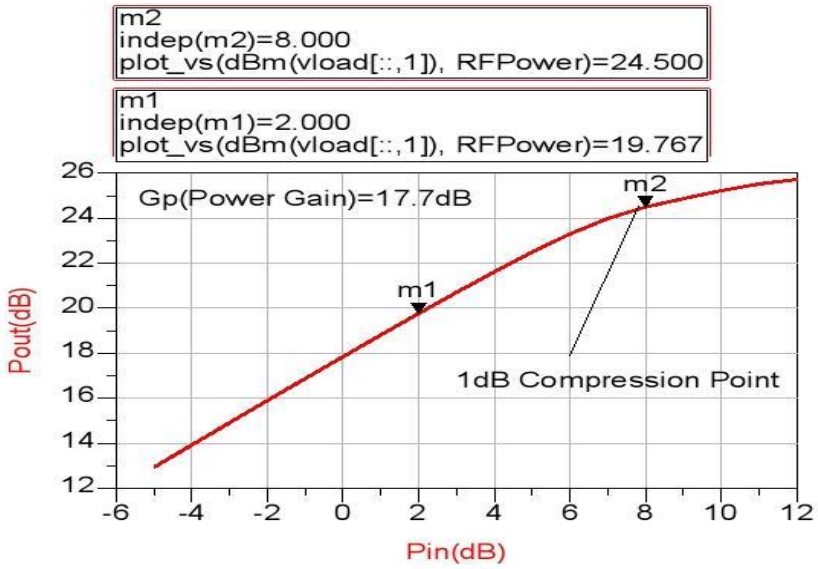

Figure 4.26-Pout versus Pin for Driver Amplifier

4.3.4 Wilkinson Power Splitter Simulation Results

The S-parameters for the power splitter show 3dB attenuation between the input and output ports. The simulation results also show 71dB isolation between the output ports.

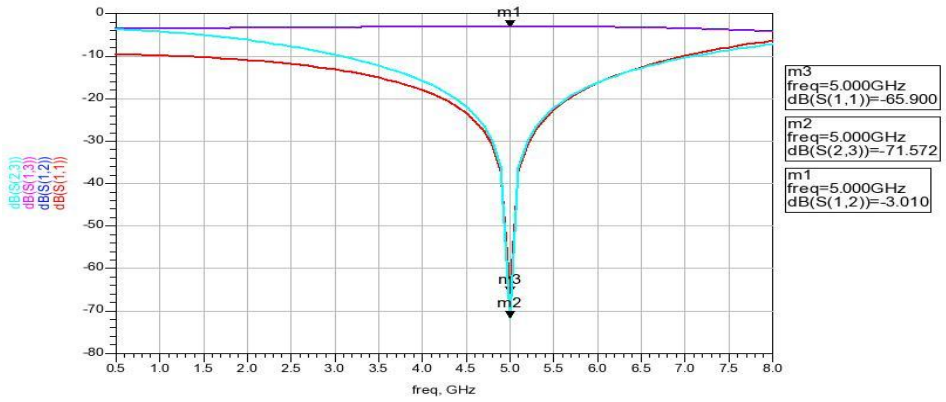

Figure 4.27-Wilkinson S-Parameters

4.3.5 3dB Attenuator Simulation Results

The schematic for the 3dB attenuator is shown above. The design equations for the circuit were presented in the previous section. The S-parameter simulation results are presented below and show 3dB attenuation over all frequencies.

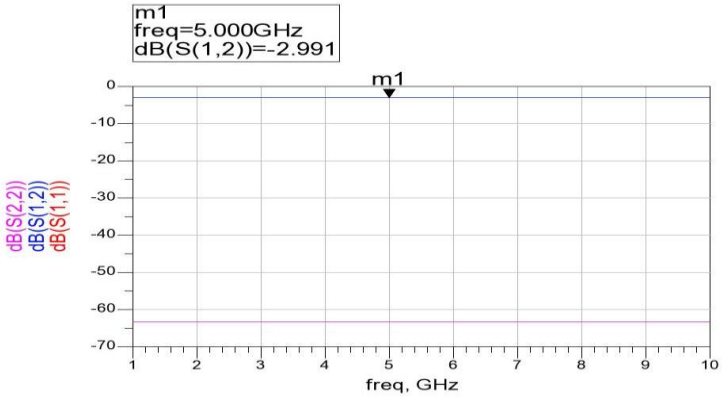

Figure 4.28-S-Parameters for 3dB Attenuator

Component Simulation Results @ Freq=5GHz

Class A Amplifier			Class C Amplifier			Driver Amplifier	
S11(dB)	-26		S11(dB)	-35		S11(dB)	-23
S12(dB)	-28		S12(dB)	-26.5		S12(dB)	-29.5
S21(dB)	10.34		S21(dB)	7.2		S21(dB)	17.98
S22(dB)	-24		S22(dB)	-9		S22(dB)	-38
Gp(dB)	10		Gp(dB)	4		Gp	17.7
PAE	45						
Wilkinson Power Splitter			3dB Attenuator				
S11(dB)	-65		S11(dB)	-63			
S12(dB)	-3		S12(dB)	-2.991			
S13(dB)	-3		S22(dB)	-63			
S23(dB)	-71.5						
S22(dB)	-65						
S33(db)	-65						

Table 4.1-Component Simulation Results

4.4 Doherty Amplifier Schematic and Simulation Results

The full schematic for the Doherty Amplifier is presented in figure 4.29.

The schematic shows the driver amplifier connected to the input port of the Wilkinson power splitter. The upper output port of the Wilkinson is driving the input to the main amplifier. The bottom output port of the Wilkinson is driving the input to the 3dB attenuator which is in turn connected to the class C auxiliary amplifier.

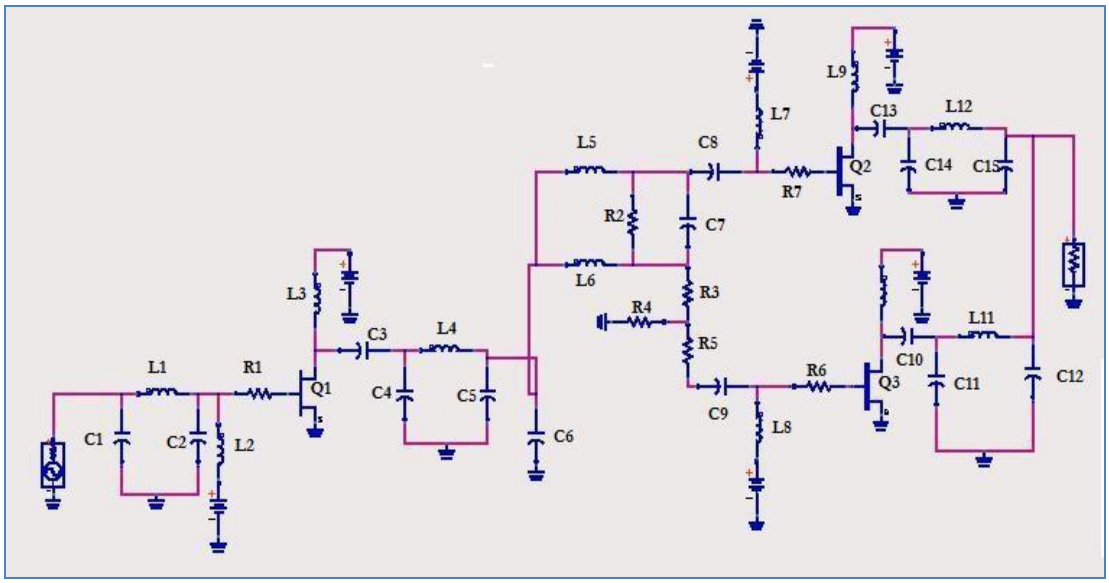

Figure 4.29-Doherty Amplifier Schematic

The S-parameters for the entire structure are presented below. The results show a power gain of 23.8 dB at 5GHz along with a reasonable input match at the operating frequency. The circuit is unconditionally stable from 300MHz up to 10GHz as shown in figure 4.31.

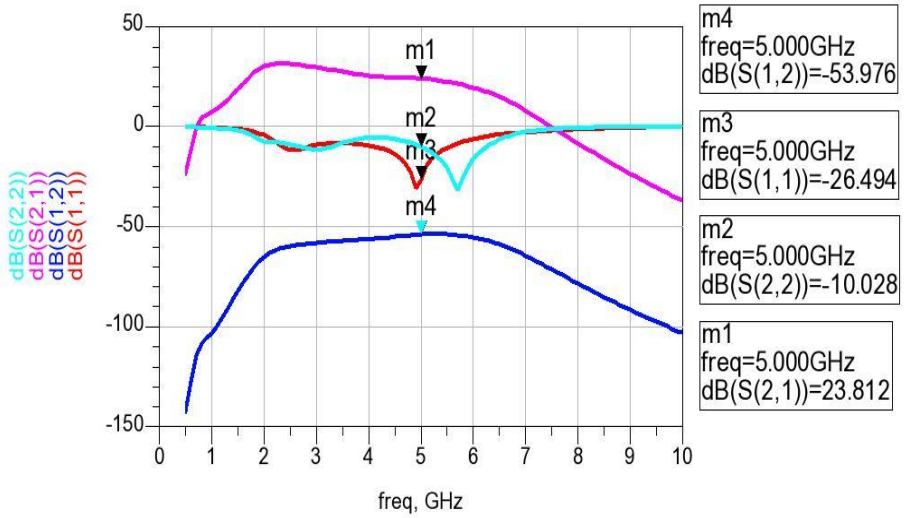

Figure 4.30-S-Parameters for Doherty Amplifier

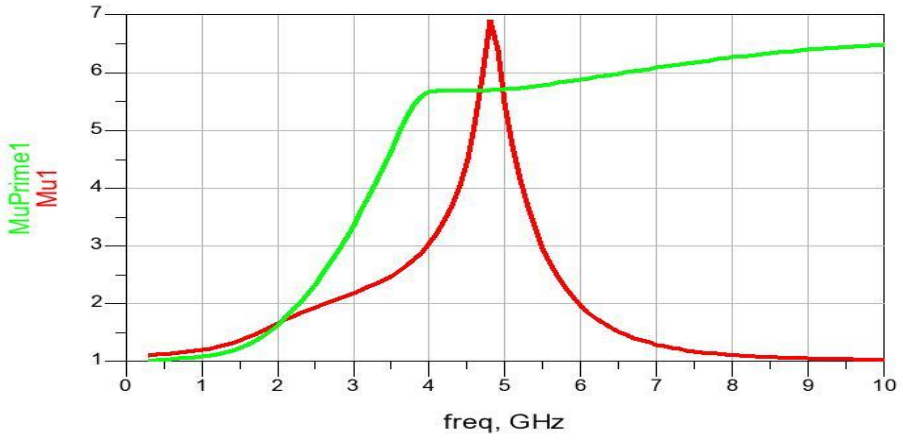

Figure 4.31-Stability Curves for Doherty Amplifier

The results of the harmonic balance simulation are presented in figures 4.32 and 4.33. Figure 4.32 shows the output power versus input power curve. The initial output power versus input power curve for the main class A amplifier starts to compress at an output power of 26dB and saturates at 28dB. Figure 4.32 shows the modified response due to active load pulling. All of the compression points

are shifted up by 3dB due to the presence of the 3dB attenuator and the auxiliary class C amplifier. Figure 4.33 shows the drain voltage of the main class A amplifier and load voltage versus time for different input power levels. As the drain voltage for the main amplifier starts, the load voltage still increases in a linear fashion due to the active load pulling effect.

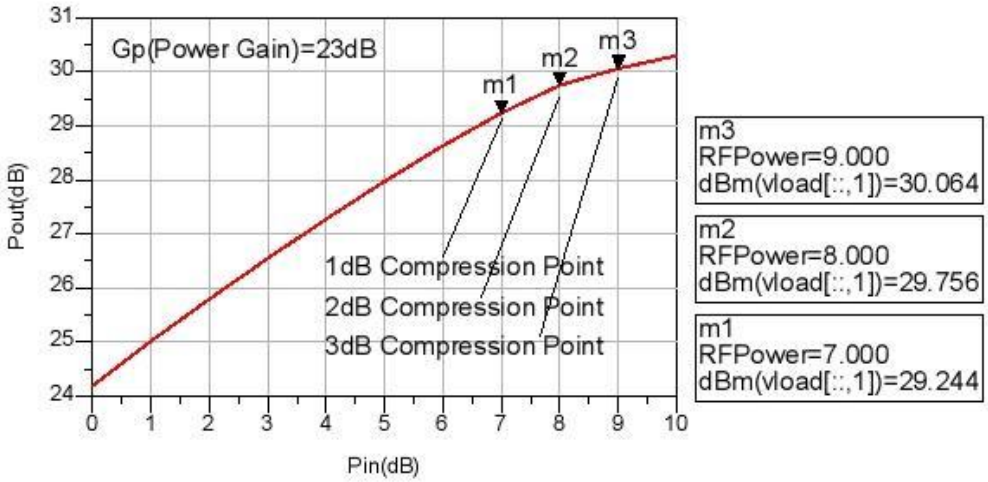

Figure 4.32-Pout versus Pin for Doherty Amplifier

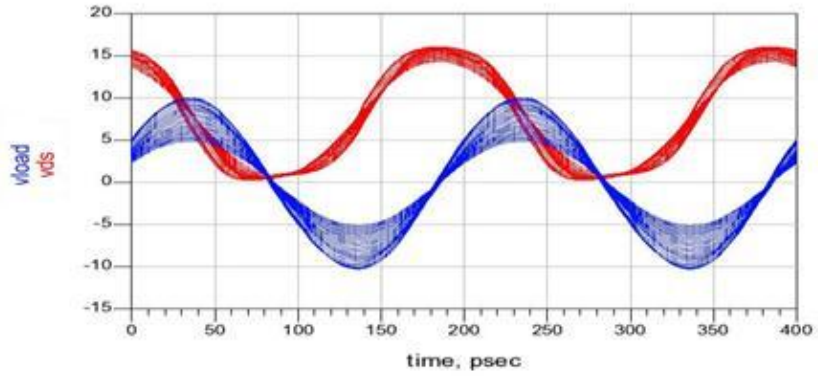

Figure 4.33-Drain and load voltages for Doherty Amplifier

Figure 4.34 shows the power added efficiency curves for the Doherty Amplifier. The power sweep curves shot that 3dB Compression starts at an input power of 9dB however the power added efficiency does not drop after this point due to the active load pulling effects.

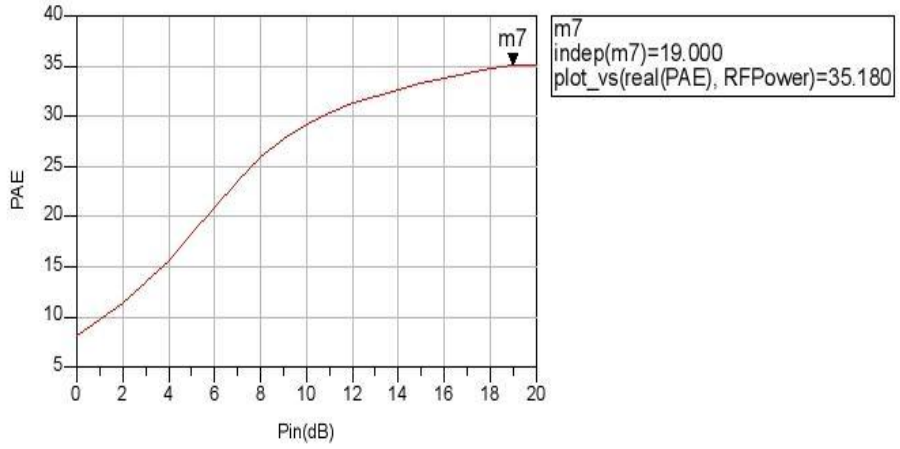

Figure 4.34-Power Added Efficiency for Doherty Amplifier

The gain linearity improvement can also be illustrated by examining two tone measurements at compression. Figure 4.35 shows the results of a two tone simulation at 3dB compression. The results show that the second intermod is 23dB below the first intermod which is very good at compression. Later, I will show test results comparing the intermod response with and without the auxiliary amplifier. These results will show a significant improvement in performance.

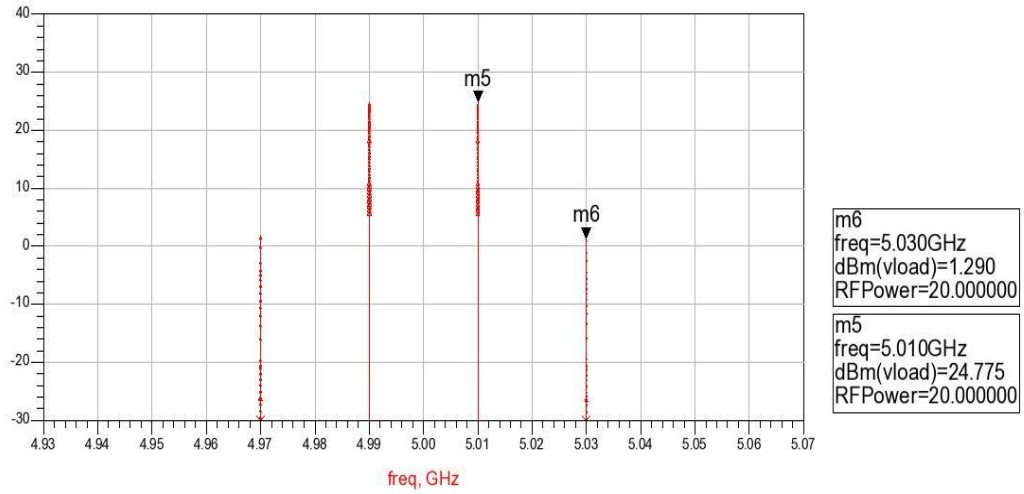

Figure 4.35-Two Tone Simulation for Doherty Amplifier

4.5 Doherty Amplifier Layout

The layout for the complete amplifier is presented in figure 4.36. The die size is 1873x1130 um^2 and the wafer thickness is 100 mils. Ground signal ground connections are place at the top and bottom of the die and the dc inputs are placed along the side. The input to the driver amp is the G-S-G connection at the bottom of the layout. The G-S-G connection at the top of the layout is the output for the amplifier.

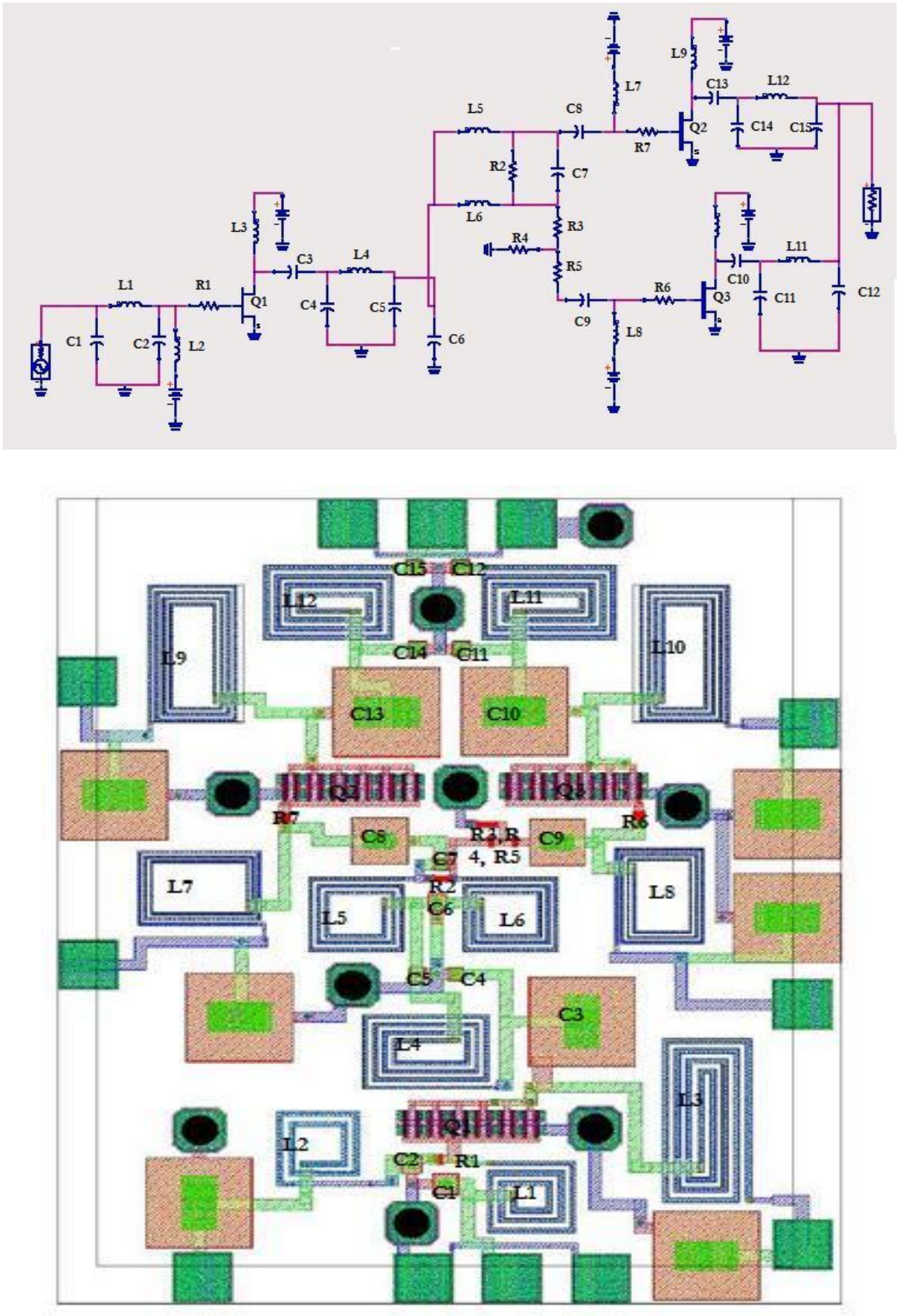

Figure 4.36-Doherty Amplifier Layout and Schematic

Schematic Label	Value	Triquent Part Type	Schematic Label	Value	Triquent Part Type
C1	1.113pF	MIM	C2	.715pF	MIM
L1	.97nH	Mrind	L2	1nH	Mrind
R1	9.5Ω	NiCr	C3	20pF	MIM
C4	.424pF	MIM	C5	.424pF	MIM
L3	3.1nH	Mrind	L4	2.387nH	Mrind
C6	.636pF	MIM	L5	1.592nH	Mrind
L6	1.592nH	Mrind	R2	100Ω	NiCr
C7	.318pF	MIM	R3	8.5Ω	NiCr
R4	142Ω	NiCr	R5	8.5Ω	NiCr
C9	5.4pF	MIM	R6	32.62Ω	NiCr
L8	2nH	Mrind	C10	20pF	MIM
C11	.53pF	MIM	C12	.53pF	MIM
L11	1.912nH	Mrind	L10	2.7nH	Mrind
C13	20pF	MIM	C14	.57pF	MIM
C15	.57pF	MIM	R7	29.1Ω	NiCr
C8	5.5pF	MIM	L9	3.8nH	Mrind
L7	2.5nH	Mrind	L12	1.847nH	Mrind
Q2,Q3	W=50um,Ng=11	PHSS	Q1	W=50um,Ng=12	EHSS

Tabel 4.2-Doherty Schematic Component Values

Figure 4.37 shows the layout for the driver amplifier. The gate bias pin is on the left and the drain bias pin is on the right. The ground signal ground connection feeds the input mathing network at the bottom of the figure. All dc pins include 20pF bypass caps.

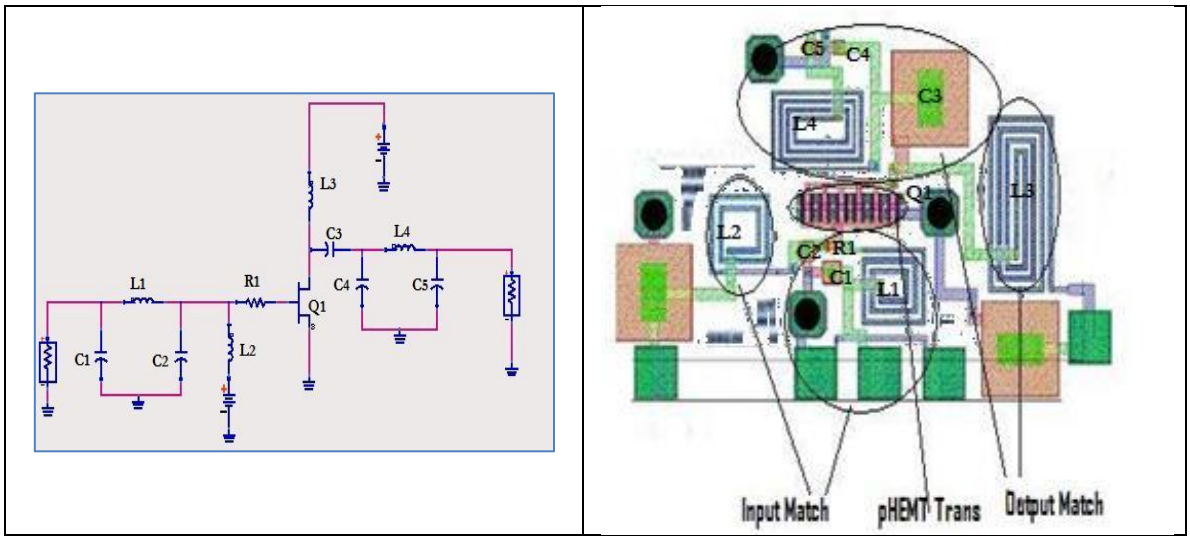

Figure 4.37-Driver Amplifier Schematic and Layout

The Wilkinson power splitter layout is presented in figure 4.38. The input to this structure is connected to the capacitor and the two spiral inductors. The outputs for this structure are connected to each spiral inductor and the parallel combination of a NiCr resistor and a MIM capacitor.

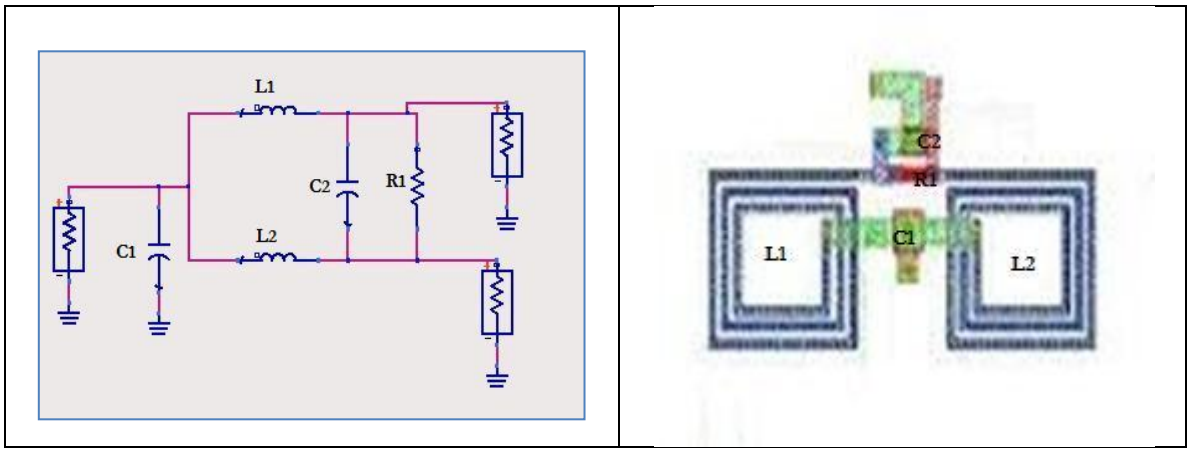

Figure 4.38-Wilkinson Layout

Figures 4.39 and 4.40 show the layout for the class A and class C amplifiers. I attempted to make the layouts as symmetrical as possible. I wanted to keep the path loss for the two amplifiers equal.

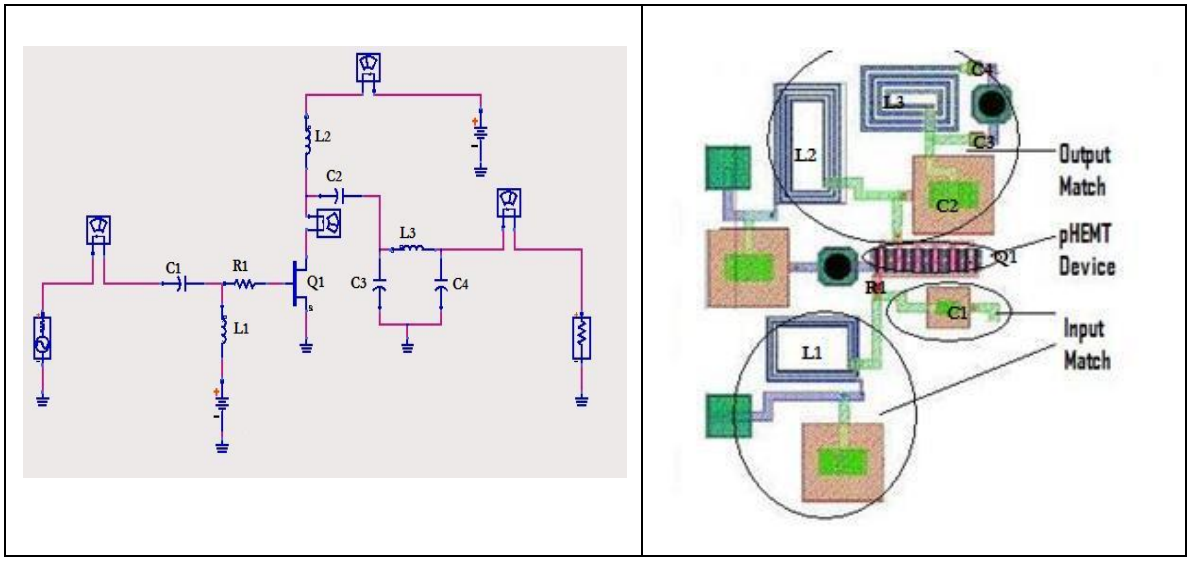

Figure 4.39-Class A Amplifier Layout

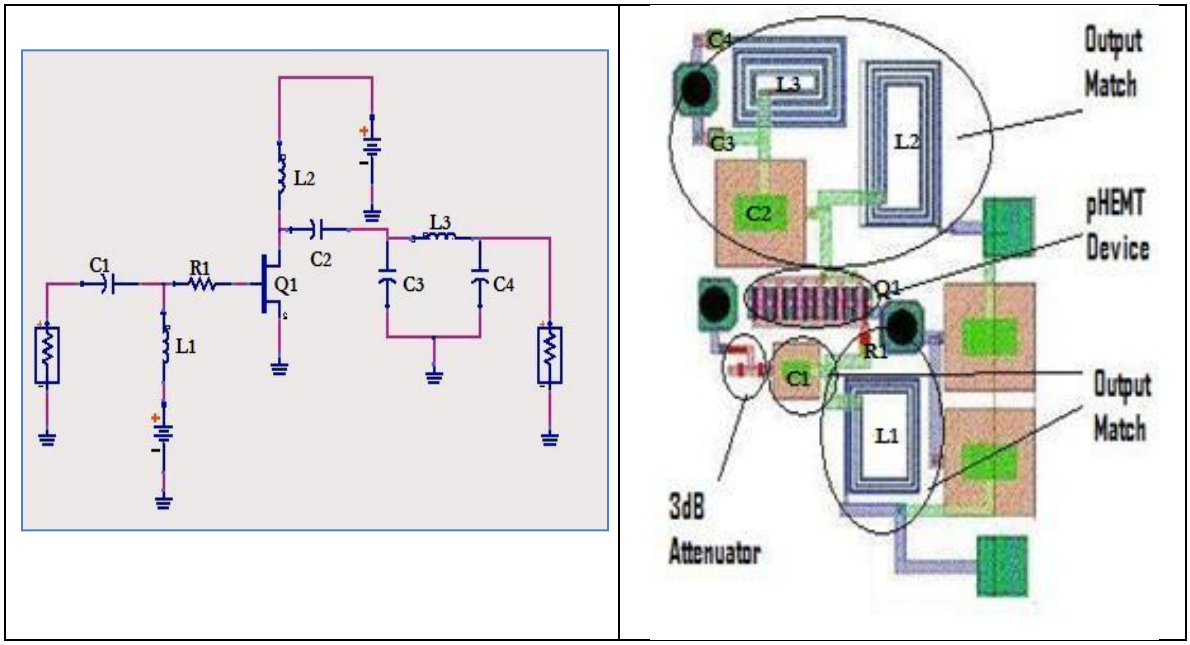

Figure 4.40-Class C Amplifier Schematic and Layout

4.6 Testing and Results

The test setup for the amplifier consisted of a 8150 Hewlett Packard network analyzer, two high frequency sources, a power meter, dc power supplies and a spectrum analyzer. The chip was mounted on a piece of metal with silver epoxy and surface mount capacitors were added to prevent low frequency oscillations. DC pins were also added for ease of testing.

The procedure for taking S-parameter measured consisted of a calibration process using a mechanical T-R-L standard over the frequency range of

interest. S-parameter measuements were taken from 300Mhz up to 10GHz using the 8150 network analyzer. The measured results show good agreement with the simulations. S_{21} is a 2 dB lower than the simulated results. S_{12} and S_{22} are also in good agreement with the simulated results. The S_{22} numbers will not reflect a conjugate match at the output since the match was optimized for output power. The S_{11} measurements are higher than expected and most likely contribute to the 2dB loss in gain.

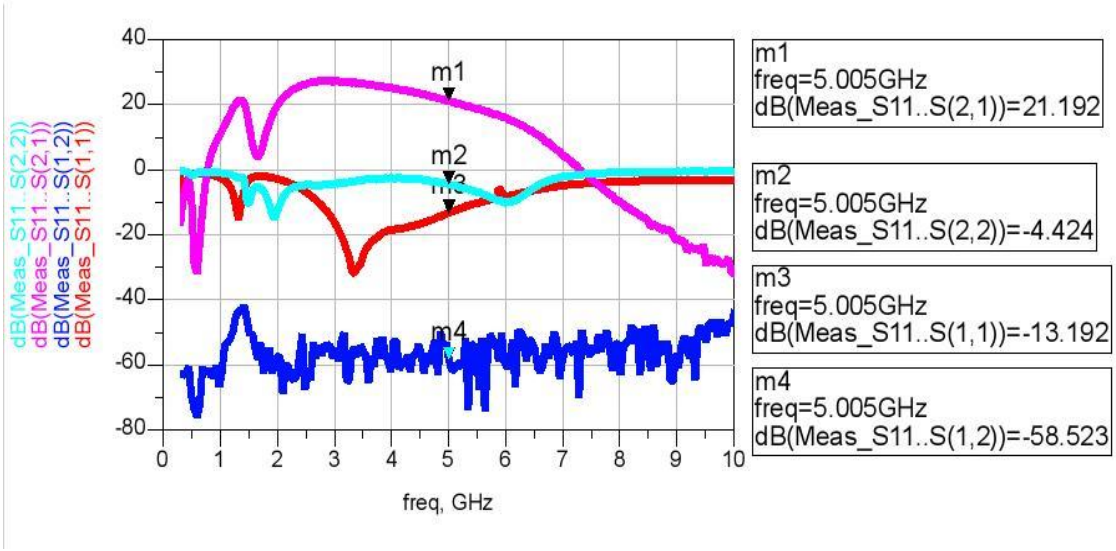

Figure 4.41-Measured S-Parameters for Doherty Amplifier

The power measurement were taken using a power meter, a high frequency source, a spectrum analyzer and a current meter. The cable losses were first

measured using a through structure and a source. The total cable loss at 5GHz a little more than 5dB. The output power for the high frequency source was verified using a power meter and a spectrum analyzer. The output power numbers were taken from the spectrum analyzer directly in order to get the power in the fundamental. The measured results show 3dBm loss in output power with respect to the simulation results.

Doherty PA

5GHz	Die#1					8V ; 240 mA			
Pin(SG)	**Pout(SA)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I1(8V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
0	-9.75	-1.83	13.85	15.68	240	1920.0	24.27	1.3	1.2
1	-8.77	-0.83	14.89	15.72	239	1912.0	30.83	1.6	1.6
2	-7.74	0.17	15.92	15.75	239	1912.0	39.08	2.0	2.0
3	-6.67	1.17	16.99	15.82	239	1912.0	50.00	2.6	2.5
4	-5.65	2.17	18.01	15.84	239	1912.0	63.24	3.3	3.2
5	-4.64	3.17	19.02	15.85	238	1904.0	79.80	4.2	4.1
6	-3.64	4.17	20.02	15.85	238	1904.0	100.46	5.3	5.1
7	-2.64	5.17	21.02	15.85	238	1904.0	126.47	6.6	6.5
8	-1.61	6.17	22.05	15.88	240	1920.0	160.32	8.4	8.1
9	-0.09	7.17	23.57	16.40	241	1928.0	227.51	11.8	11.5
10	-0.41	8.17	23.25	15.08	244	1952.0	211.35	10.8	10.5
11	1.36	9.17	25.02	15.85	244	1952.0	317.69	16.3	15.9
12	2.28	10.17	25.94	15.77	250	2000.0	392.64	19.6	19.1
13	3.03	11.17	26.69	15.52	250	2000.0	466.66	23.3	22.7
14	3.57	12.17	27.23	15.06	257	2056.0	528.45	25.7	24.9
15	4	13.17	27.66	14.49	262	2096.0	583.45	27.8	26.8
16	4.38	14.17	28.04	13.87	265	2120.0	636.80	30.0	28.8
17	4.63	15.17	28.29	13.12	271	2168.0	674.53	31.1	29.6
18	4.74	16.17	28.40	12.23	274	2192.0	691.83	31.6	29.7
19	4.82	17.17	28.48	11.31	276	2208.0	704.69	31.9	29.6
20	4.87	18.17	28.53	10.36	276	2240.0	712.85	31.8	29.3

Table 4.3-Measured Pout versus Pin and PAE Results

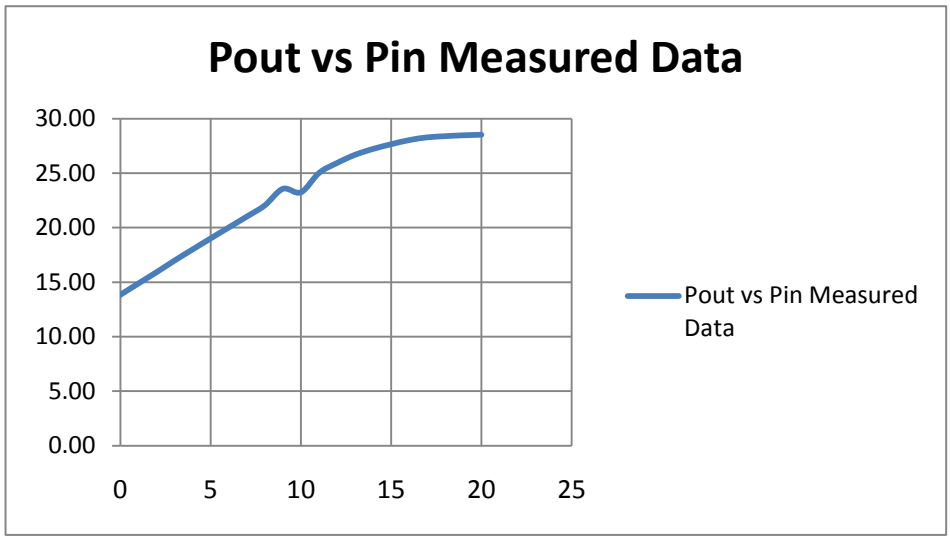

Figure 4.42-Pout versus Pin Measured Data

The setup for the two-tone measurements is the same as the power measurements except an additional high frequency source and a power combiner were used. The sources were set to 4.9GHz and 5.1Ghz for the measurement. The input power levels were swept and the first intermod was measured .The measurements were taken with and with out the auxillary amplifier. The measured results show a 10dB decrease in intermod levels when the auxillary amp is used with the main amplifier. The intermod levels increase as the amplifiers get close to compression. The results show that the Doherty configuration gives a 6dB improvement in output power before the intermod levels increase to an undesirable level.

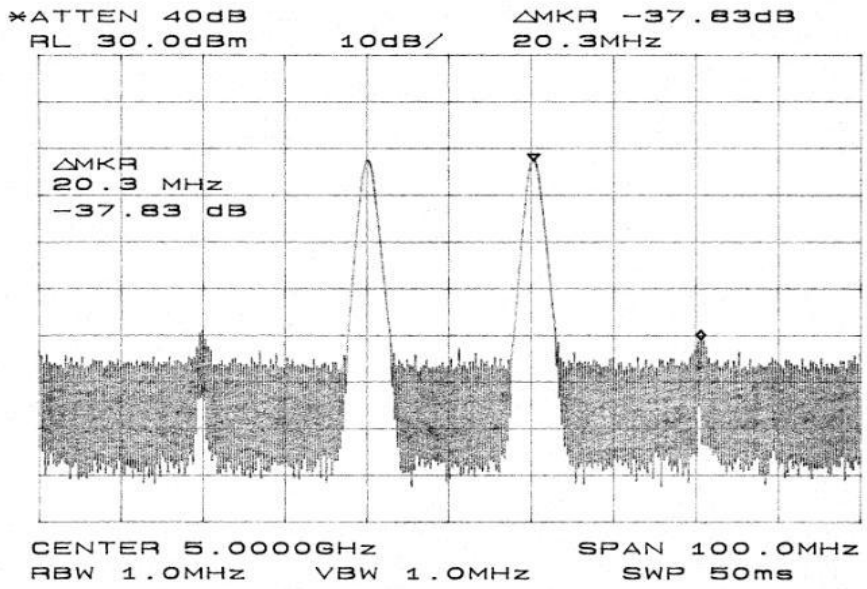

Figure 4.43-Two Tone Meas. of Doherty without Auxiliary Amplifier @ Pout=8dB

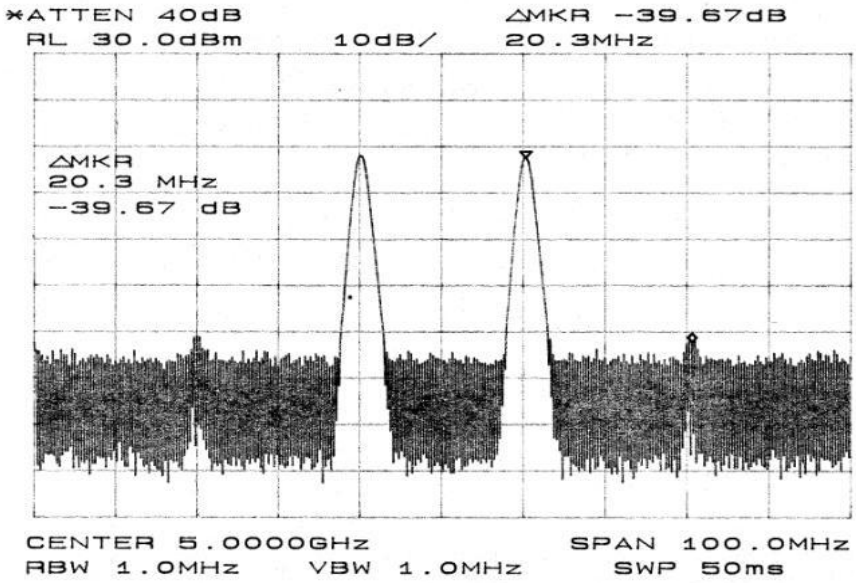

Figure 4.44-Two Tone Meas. of Doherty Amp with Auxiliary Amplifier @ Pout=8dB

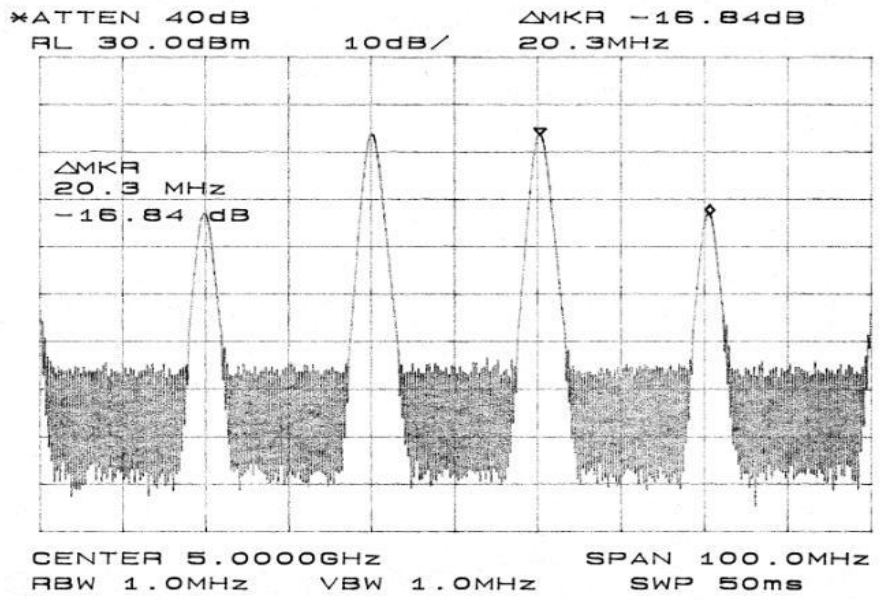

Figure 4.45- Two Tone Meas. of Doherty without Auxiliary Amplifier @ Pout=13.5dB

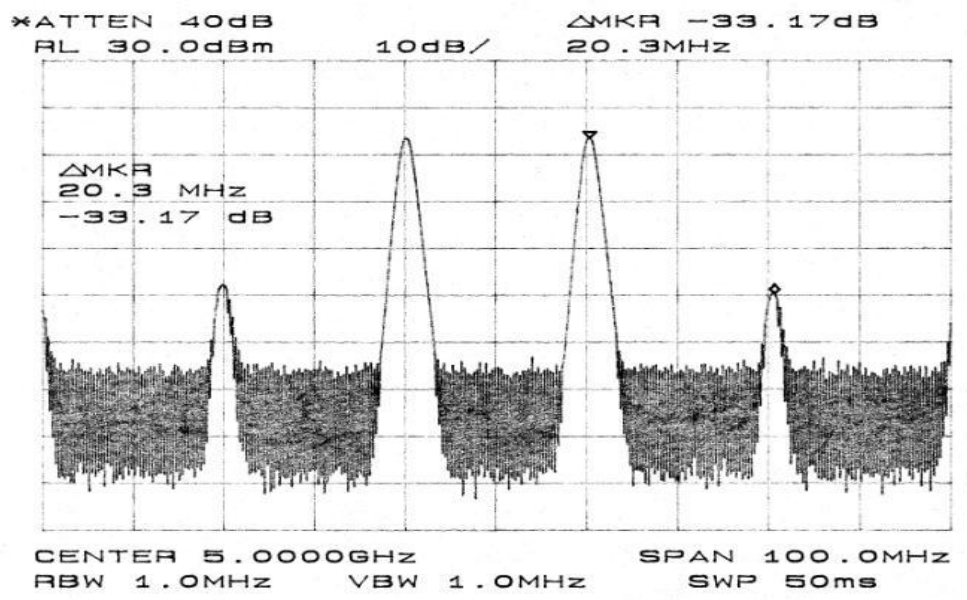

Figure 4.46-Two Tone Meas. of Doherty with Auxiliary Amplifier @ Pout=13.5dB

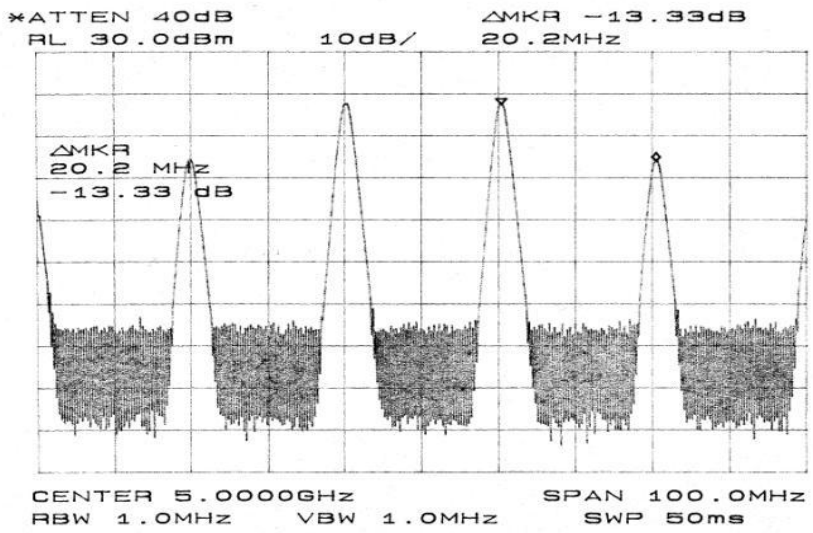

Figure 4.47-Two Tone Meas. of Doherty with Auxiliary Amplifier @ Pout=18dB

Doherty Amplifier Results

Simulated				**Measured**	
S11(dB)	-26.5			S11(dB)	-13.2
S12(dB)	-54			S12(dB)	-58
S21(dB)	23.8			S21(dB)	21.192
S22(dB)	-10			S22(dB)	-4.4
Gp(dB)	23			Gp(dB)	15.8
PAE	35			PAE	29.6
Pout Max(dB)				Pout Max(dB)	
	30				28.5
Intermod w/o Auxiliary Amp				**Intermod w/ Auxiliary**	
Pout=8dB				**Pout=8dB**	
IM(dBc)	-37.8			IM(dBc)	-39.67
Pout=13.5dB				**Pout=13.5dB**	
IM(dBc)	-16.84			IM(dBc)	-33.17
				Pout=18dB	
				IM(dBc)	-13.33

Table 4.4-Doherty Amplifier Measured versus Simulated Results

4.7 Discussion

The measured S-parameter results show a fair match to the simulated results with the exception of S_{11}. The measured results are 13dB higher than the simulation results. The smith chart representation of the measured S_{11} result shows a positive reactive part and a real part that is slightly lower than 50 Ohms. The added reflections at the input partly explain the 2dB S_{21} drop. These added reflections do not explain the 8dB loss in large signal gain and 3dB loss in output power. I believe that the die does not have sufficient heat dissipation. The die is consuming close to 2Watts of power with a large heat sink. Furthermore, I did not have enough room in the setup for a fan. I repeated the power measurements several times with the same result. I also noticed some minor damage to the passivation and reduced output power with repeated measurement. I did manage to see a significant improvement in the inter-modulation response when the auxiliary amplifier was used. The simulations showed that the PAE numbers did not decrease after 3dB compression and the Measurements confirmed this. Finally, the simulated and measured results for PAE are poor. I believe that the driver amplifier is responsible for this. I designed that stage for testing purposes only. If I could somehow decouple that

stage from the rest of the design, I think the PAE numbers would be closer to the simulated results for the Class A amplifier.

Chapter 5: Conclusion and Future Work

5.1 Conclusion

The Doherty amplifier configuration is one method to achieve both reasonable efficiency and good gain linearity. The class A amplifier performance can be improved upon by using load pulling to extend the linear region without paying too much of a penalty in efficiency. The goal of this research was to implement a Doherty Amplifier at 5GHz with all of the matching and power combining circuitry on a single chip. Through careful design, implementation, and measurement, this goal has successfully been achieved. The Doherty Amplifier created in this thesis operates at 5 Ghz with a maximum output power of 28dBm and a Power Added Efficiency of 29.6 percent. The work in this thesis reinforces the notion that the Doherty configuration is a viable method to achieve both reasonable efficiency and good gain linearity. It serves as a first ever implementation of the Doherty configuration at 5 Ghz on a single chip.

Two problems were encountered during this thesis work. The first was that the measured input match of the amplifier was lower than initially simulated, a difference of 13 dB was found. Secondly the output power was 2 dBm lower than the simulations. These two problems are largely due to self-heating of the

transistors and slight differences in the model from the actual devices. Given more resources, these problems could be easily corrected.

While the design was successful, several enhancements could be made to the design to extend its linear range. Through the research done and described in this thesis, it has been shown that the inter-modulation response of the amplifier can be improved by adding one stage of active load pulling. In addition the linear range of the amplifier could also be extended by adding more class C active load pulling stages with different attenuation levels.

5.2 Future Work

Future Doherty Amplifier research will focus on a few key areas. The first area will be extending the linear range of the power gain. This can be accomplished by increasing the number of auxiliary amplifiers and attenuators used in the circuit. The attenuator values can be staggered such that the auxiliary amplifier can cut on as the preceding auxiliary amplifier saturates.

The second area of research should focus on linearizing the phase response of the Doherty Amplifier. As the output of the Class A Amplifier starts to compress, the input signal experiences a phase shift as it is amplified. The phase shift is non-linear in nature and is not desirable in communications systems. All

of the research on Doherty Amplifiers has focused on narrow band signals. The third and most challenging area of research will focus on extending the bandwidth of the Doherty structure to accommodate use in OFDM systems.

A reasonable and challenging bandwidth goal would be a full octave in the 5 GHz range. Research in these three areas: auxiliary amplifier addition, improved phase response, and octave wide bandwidth research would provide further proof of the robustness of the Doherty Amplifier architecture and make it a serious consideration for future device designers.

References

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